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Encounter Conformal Low Power

Fast and accurate creation, verification, and integration of power intent

Cadence® Encounter® Conformal® Low Power enables engineers to verify and debug multimillion-gate designs optimized for low power, without complex and time-consuming gate-level simulations. It also enables the creation, validation, and integration of power intent in the context of the design. By combining low-power structural and functional checks with world-class equivalence checking, Conformal Low Power provides superior performance, full-chip capacity, and ease of use.

Encounter Conformal Technology

To shorten overall design cycle times and minimize silicon re-spins, designers need production-proven validation tools. Encounter Conformal verification technologies offer the most comprehensive and trusted solutions for equivalency checks, timing constraints management, clock-domain-crossing synchronization checks, analysis and generation of functional engineering change orders (ECOs), and low-power design optimization and verification.

Encounter Conformal Low Power

Optimizing for leakage and dynamic power helps designers reduce energy consumption and it lowers packaging costs. While advanced low-power methods—such as static and dynamic voltage and frequency scaling, power gating, and state retention—offer additional power savings, they also complicate the verification task.

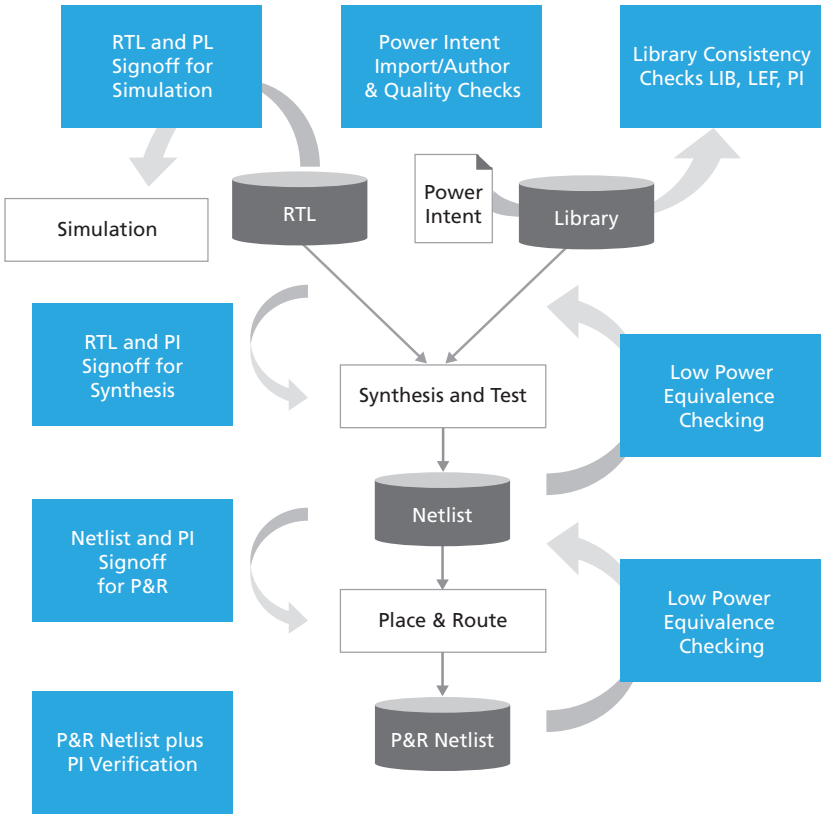

Figure 1: Low-power verification flow with Encounter Conformal Low Power

Verification complexity is amplified by the fact that the majority of the low-power function is introduced into the gate netlist during synthesis and physical implementation. Most simulation-based verification takes place at the RTL. Full-chip, gate-level simulation is neither a practical nor scalable methodology for verifying the logic function of today's designs due to their size and complexity.

Encounter Conformal Low Power address these challenges. It combines proven equivalence checking, structural and functional checks, and formal techniques to enable full-chip, low-power optimization and verification. Encounter Conformal Low Power is available in XL and GXL offerings.

Benefits

- Minimizes silicon re-spin risk by providing complete verification coverage
- Detects low-power implementation errors early in the design cycle
- Speeds identification of low-power design problems through a single unified cockpit for debugging power intent, RTL, logical netlist, and physical netlist power issues
- Verifies multimillion-gate designs faster (by orders of magnitude) than traditional gate-level simulation
- Closes the RTL-to-layout verification gap
- Decreases risk of missing chip-killing bugs through complete formal checks that leverage independent verification technology
- Helps power architects create, validate, and integrate power intent in context of the design
- Delivers the industry's most trusted solution for low-power verification

Features

Encounter Conformal Low Power XL

The XL configuration combines logic equivalence checking for the most complex low-power SoC and datapath-intensive designs, with functional and structural checks for low-power designs.

Power intent creation, verification, and debug

For a moderate design with only a few power domains, creating power intent in a text editor may be relatively simple. But as designs employ more elaborate power saving techniques, creating them in a text file can be difficult and error-prone.

Conformal Low Power allows you to create power intent in the context of the design and libraries. You may define macro models for IP or a level of hierarchy, describing internal power characteristics of blocks. Macro modeling is key to enabling higher levels of design abstraction. The power intent integration feature can merge and resolve hierarchical power intent and generate a single, top-level set of power specifications. Conformal Low Power can read/write power intent to a file. At any point in the design process, running power intent quality checks will catch any syntactical and semantic issues. Cross-probing between error/warning messages, the design source (RTL/gate netlist), and the power intent file will speed debug of these issues and the refinement of power intent.

Conformal Low Power provides independent verification of low-power designs in flows with a mixture of simulation, synthesis, and physical implementation tools. Likewise, it supports an interoperable environment for power intent based on an interoperable subset of the power intent formats.

Equivalence checking

During development, a low-power design undergoes numerous iterations prior to final layout, and each step in this process has the potential to introduce logical bugs. Conformal Low Power checks the functional equivalence of different versions of a low-power design at these various stages and enables you to identify and correct errors as soon as they are introduced. For example, it validates post-synthesis netlist and instantiated power intent back against the verified-golden

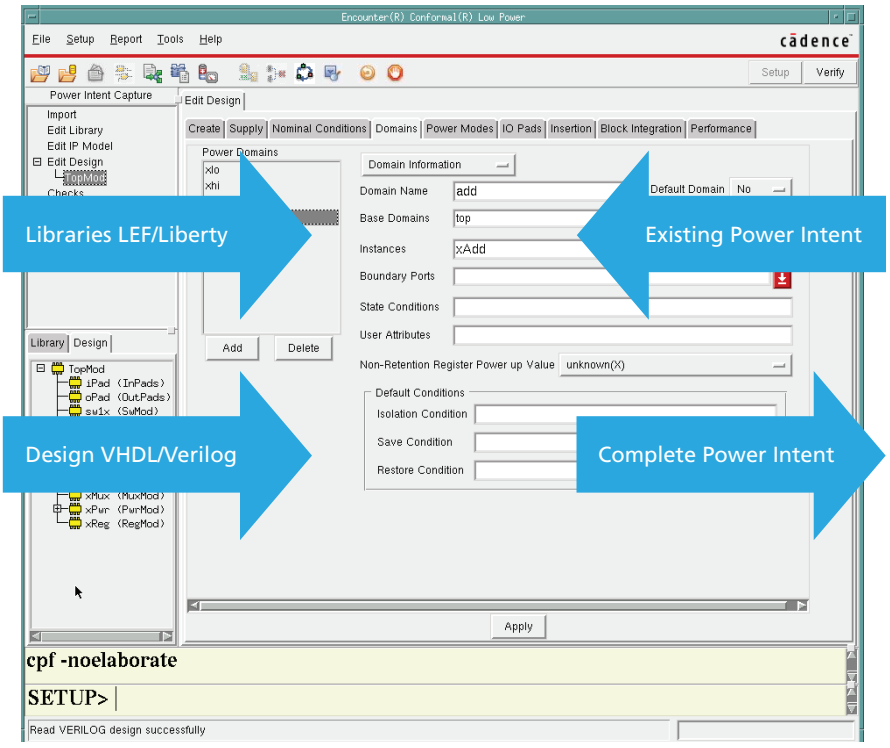

Figure 2: Power intent authoring speeds power intent capture and debug

RTL and its associated power intent. It supports advanced dynamic and static power synthesis optimizations such as clock gating and signal gating, multi-Vt libraries, and de-cloning and re-cloning of gated clocks during clock tree synthesis and optimization.

Conformal Low Power supports the Common Power Format (CPF) specification language. It uses CPF for guidance to independently model how implementation inserts and connects low-power cells—level shifters, isolation, and state retention registers—into an RTL design, thus enabling true low-power equivalence checking from RTL to the gate level. Conformal Low Power can also model level shifters and isolation cells as domain anchor points during equivalence checking to detect whether logic gates have erroneously crossed domain boundaries from one version of the netlist to another. Conformal Low Power supports other power intent standards as well.

Structural and functional checking

Conformal Low Power supports multi-supply voltage (MSV) islands, coarse-grain power gating (PSO), coarse-grain ground switching (GSO), dynamic voltage and frequency scaling (DVFS), and state retention power gating design techniques. It can also perform power domain structural and functional checks on an RTL design with CPF, a logical gate netlist (typically post-synthesis), and a power-aware physical gate netlist (after place-and-route).

For RTL and logical gate netlist checking, you define the power intent: power domains, ground domains, voltages, standby conditions, power modes, and power associations along with the low-power cells being used. Conformal Low Power then propagates the domains throughout the design hierarchy and identifies all domain boundary crossings. Finally, it reports:

- Power and ground domain assignment-related problems and floating connections
- Level shifters: missing, redundant, wrong domain location, or wrong connectivity
- Isolation cells: missing, redundant, wrong gate type, wrong location, wrong isolation enable polarity
- Control signals that are not powered appropriately

Conformal Low Power supports dedicated and non-dedicated isolation cells, as well as combination isolation and level-shifter cells. It also performs isolation and state retention functional checks using formal methods.

For physical netlist checking, Conformal Low Power accepts a Verilog power-aware netlist and simulation or Liberty models. It uses top-level power pins, power and ground nets, power switches (MTCMOS), ground switches, island voltages, power pin associations, and low-power cells to automatically derive the power domains and domain crossings in the design. The entire tool set-up for physical netlist checking can also be derived from CPF. Actual physical netlist support is unique to Conformal Low Power—it analyzes the design with real power connectivity, not assumed connectivity based on instance name. Conformal Low Power reports:

- Incorrect power and ground connectivity, including shorts and opens
- Instances with undefined power domains or mixed power domains
- Missing, redundant, and incorrect power connection and wrong level-shifter types
- Missing, redundant, and incorrect isolation cell power connectivity
- Power control signals to power switches, isolation cells, and state retention registers that are not powered
- Incorrect power connection to state retention registers

Conformal Low Power also performs isolation functional checks on user-defined isolation cells, as well as standard cell-based isolation. It also runs sleep and wake sequence functional checks on state retention registers using formal methods.

Integrated environment

An intuitive and interactive GUI simplifies set-up and debugging, allowing you to quickly operate the tool and pinpoint the cause of failed checks. Included are:

- Graphical debugging via an integrated schematic viewer
- Automatic error candidate identification for equivalence checking with assigned and weighted percentages
- A Low-Power Manager GUI that helps you debug failed checks
- Waveform viewing and automatic counter-example generation for failed isolation and state retention properties

Encounter Conformal Low Power GXL

The GXL configuration includes all the features of Encounter Conformal Low Power XL and adds support for transistor circuit analysis, abstraction, and equivalence checking for custom designs, standard cell libraries, I/O pads, and embedded memories. It also offers unique checks for circuit integrity, such as drive strength checking via the transistor stacks, and checking for circuit problems across power domain boundaries such as sneaky DC paths during power down.

Conformal Low Power GXL can also abstract from a transistor cdl/SPICE netlist accurate power-aware Verilog models of level shifters and isolation cells. This allows you to identify inconsistencies among simulation, Liberty, SPICE, and LEF models. It can also help validate that the isolation cells used in the low-power design are appropriate.

Platforms

- Linux (32-bit, 64-bit)
- Sun Solaris (64-bit)
- HP-UX (32-bit, 64-bit)
- IBM AIX (32-bit, 64-bit)

Languages

- CPF 1.0, 1.1
- Mixed language:
  - Verilog (1995, 2001)
  - SystemVerilog
  - VHDL (87, 93)
  - SPICE (traditional, LVS)
- Liberty

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- Cadence application engineers can answer your technical questions by telephone, email, or Internet—they can also provide technical assistance and custom training
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