cadence®

Joules RTL Power Solution

Unified power calculator for accurate RTL power and signoff-quality gate power

Getting an accurate measure of RTL power consumption during design exploration has long been a major challenge for SoC design teams. Another challenge is getting consistent power through the design progress from RTL to P&R, because different tools are used at different stages of the design. System-level verification tools have the capacity to exercise real use cases but they are disconnected from the implementation tools that translate RTL to gates and wires.

Overview

The Cadence® Joules™ RTL Power Solution closes this gap by delivering time-based RTL power analysis with system-level runtimes and capacity, as well as high-quality estimates of gates and wires based on production implementation technology.

The Joules solution also integrates seamlessly with the Cadence Palladium® emulation platform and the Stratus™ High-Level Synthesis (HLS) platform for early system-level power analysis and optimization.

Figure 1: Joules RTL Power Solution correlation to Voltus signoff power across real customer designs

Key Features and Benefits

- 20X faster time-based power analysis using a multi-threaded frame-based architecture

- Single power calculator for different levels of design abstraction—RTL, gate level, SoC, and block level

- 20 million instances overnight using a natively integrated prototype synthesis

- 15% accuracy to signoff in the Cadence Voltus™ IC Power Integrity Solution with unified power calculation and advanced RTL-to-gate name mapping

- Seamless integration with Palladium Dynamic Power Analysis (DPA) solution with native read and write to/from Palladium PHY database

- Seamless integration with Cadence Incisive® Enterprise Simulator with native read and write to/from .SHM database

- Fast incremental "what-if" power analysis across different frequencies

- Concurrent power analysis across multiple stimulus files

- Merging of multiple stimulus files across different design hierarchies into a chip-level power view

- Ability to "zoom in" on peak power frames with increasing resolution

- Rich set of customizable power-analysis utilities at the word level and bit level

- Advanced library profiling utilities

- RTL or gate-level VCD, Palladium PHY, SAIF, or TCF input file formats

- RTL or gate-level SAIF or TCF export
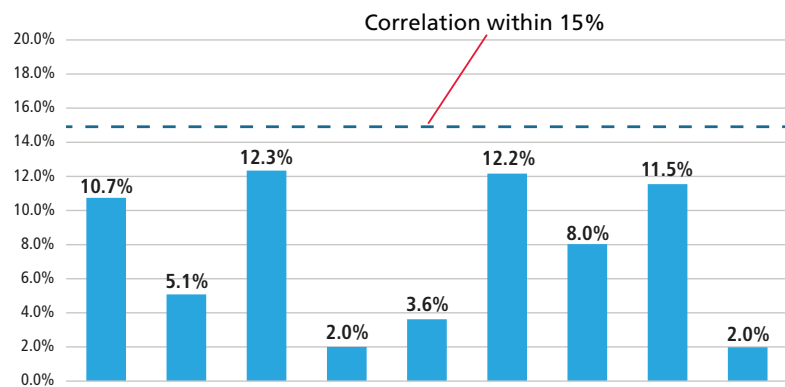
- Forward SAIF generation

Multi-Threaded Frame-Based Architecture

Power analysis is parallelized across multiple CPUs, accelerating in-depth power exploration. Multiple stimulus files can be analyzed simultaneously and each stimulus file can be time-sliced into frames to enable time-based power reporting.

Accurate RTL Power Estimation

The Joules RTL Power Solution performs an ultra-fast design synthesis using a new integrated prototype mode of the Cadence Genus™ Synthesis Solution, including physically aware clock tree and datapath buffering.

Single Power Calculator for Entire Design Flow

The Joules RTL Power Solution can also compute power accurately on a gate-level netlist and correlate to within 2-5% of signoff power.

Adjustable Power Analysis Resolution

Power-critical frames of a large system-level simulation can be zoomed in on with increasing resolution to identify the correct narrow time slice for IR-drop and thermal signoff. Full gate-level-accurate SAIF or TCF can be exported for this identified narrow time slice only for use in power signoff.

Advanced Data Mining and Debug

Power can be reported at the bit level or register level, and can be categorized based on logic cell type, power category, design hierarchy, clock domain, power domain, or timing mode. A rich suite of library analysis tools is also included, which allows profiling of cells by drive strength versus area or delay or power.

Hardware-Accelerated System-Level Power Analysis

The Joules RTL Power Solution can be invoked directly from within the Palladium DPA solution GUI, where it can natively report time-based power waveforms.

SystemC-Level Power Analysis

The Stratus HLS platform is able to automatically leverage the Joules solution during high-level synthesis to provide SystemC®-level power profiling and performance versus power tradeoff dashboarding.

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