cadence®

Cadence Physical Verification System

In-design and back-end physical verification for faster final signoff

Proven on many successful production tapeouts in nanometer process technologies, Cadence® Physical Verification System is the premier Cadence signoff solution enabling in-design and back-end physical verification, constraint validation, and reliability checking. It offers competitive distributed processing performance for advanced nodes, and its file compatibility and ease-of-use make it a drop-in replacement for existing physical verification technologies. Designed to preserve design intent, ensure design convergence, and deliver a predictable debug cycle, Cadence Physical Verification System provides a faster path to final signoff.

Cadence Physical Verification System

Cadence Physical Verification System (PVS) integrates with industry-standard Cadence Virtuoso® custom/mixed-signal and Cadence Encounter® digital design flows. This provides designers with an end-to-end design and signoff solution from a single vendor.

PVS is a trusted solution that enables users to achieve advanced node design signoff in a quick total turnaround time. It provides efficient, effective debug tools to reduce debug time and increase productivity. This solution supports advanced process node technology (such as double patterning, 3D-IC, and advanced device extraction), and it extends physical verification technology into design reliability checking and constraint validation. PVS also offers a distributed multi-threading processing capability that greatly accelerates throughput without requiring specialized hardware.

Seamless integration with the Virtuoso platform

As an integrated component, Physical Verification System works seamlessly within the Virtuoso custom IC design platform. Through interactive mode, PVS provides dynamic and real-time signoff design-rule checking (DRC) for every edit. Through in-memory/batch full-signoff verification mode, PVS can directly read in design data from the Virtuoso environment, which eliminates redundant Pcell evaluation and stream out. PVS can rapidly check the design to maximize productivity with what-if analysis. The results can be viewed and debugged with either the Virtuoso Annotation Browser or with the PVS Results Manager. Intuitive PVS debug tools (Interactive Short Locator and Graphical LVS Debug) are available in the Virtuoso platform. They can verify designs by using the technology constraints, design constraints, and signoff rule deck.

In-line integration with the Encounter platform

Within the Encounter digital implementation platform, PVS can interactively verify the design by directly accessing Encounter data and standard cell data from the OpenAccess database. This means designers can invoke PVS and browse its error

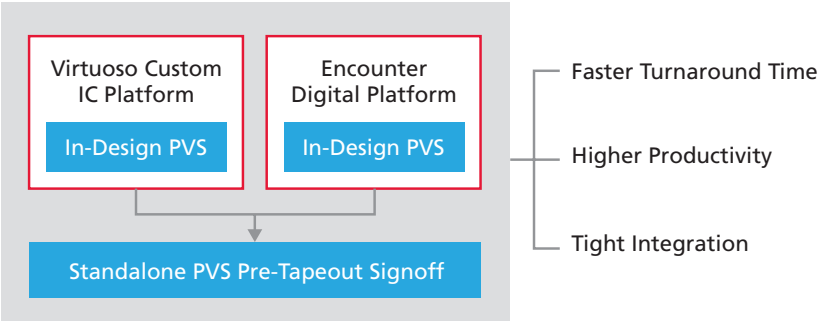

Figure 1: Used either in-design or standalone, PVS enables efficient design, implementation, and foundry signoff closure

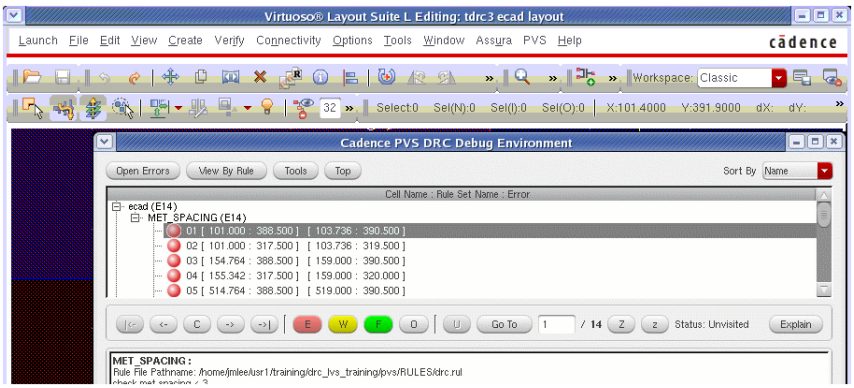

Figure 2: The Virtuoso GUI displays the DRC debug environment

markers without converting data from the Encounter design environment. Using PVS, they can generate regular metal fill and advanced timing-aware metal fill using the signoff rule file. Designers can launch the PVS Results Manager and intuitive debug tools within the Encounter design environment.

Benefits

- Trusted solution with production-proven accuracy
- Single-vendor solution for implementation and pre-tapeout signoff
- Quick turnaround time from design to signoff through integration with Virtuoso and Encounter design flows
- Innovative technology to support advanced process node design
- Reduced debug time with powerful and intuitive debugging tools
- Simplified migration through compatibility with industry-standard formats
- Cost-effective parallel computing systems, eliminating the need for hardware modifications

Features

Interactive and batch verification

Physical Verification System (PVS) works for both interactive and batch modes. Interactive physical verification, integrated within the Virtuoso and Encounter platforms, helps designers preserve design intent to ensure design convergence. PVS also operates in DFII and OpenAccess environments. Furthermore, PVS integrates seamlessly with Cadence QuickView Layout and Manufacturing Data Viewer. It also runs standalone to verify the finished chip.

Virtuoso DRC

Traditional DRC use models involve packaging up the layout (i.e. GDSII) and invoking a DRC run. This requires the data preparation, launching of the job, and then pushing any error data/markers back into the layout view. Virtuoso DRC is a new capability that integrates PVS DRC technology with Virtuoso Layout Suite in a real-time mode. This convenient use model enables layout designers to run DRC using a signoff-level DRC deck as they complete each edit.

Layout designers can also leverage this technology to do interactive editing checks by using the OA tech file. Full signoff verification can be done at the block and chip levels by using the fully foundry-qualified signoff deck, and it can be run from Virtuoso memory space. Using Virtuoso DRC, layout designers can perform design, implementation, and in-memory signoff checks within the Virtuoso environment. With correct-by-construction and dynamic detection/verification of the editing geometries, this DRC technology speeds turnaround time, brings signoff confidence to layout designers, and ultimately improves design quality.

Programmable Electrical Rule Checker

The PVS Programmable Electrical Rule Checker (PERC) reduces the risk of low reliability and provides a platform to translate the designer's intent into a set of rules. The PERC uses the designer's rules throughout the whole development process, at pre- and post-layout stages. It identifies the place with high reliability risk in the early stage of development, and it checks that the solution used to reduce reliability risk satisfies the designer's netlist-based and layout-based requirements.

The PVS PERC can be applied to find ESD unprotected devices and pads, to check the ESD protection structure, and to find cross-power domain interface structures and check them. The PERC can be used to find common errors (such as floating gates or prohibited power domains) in the

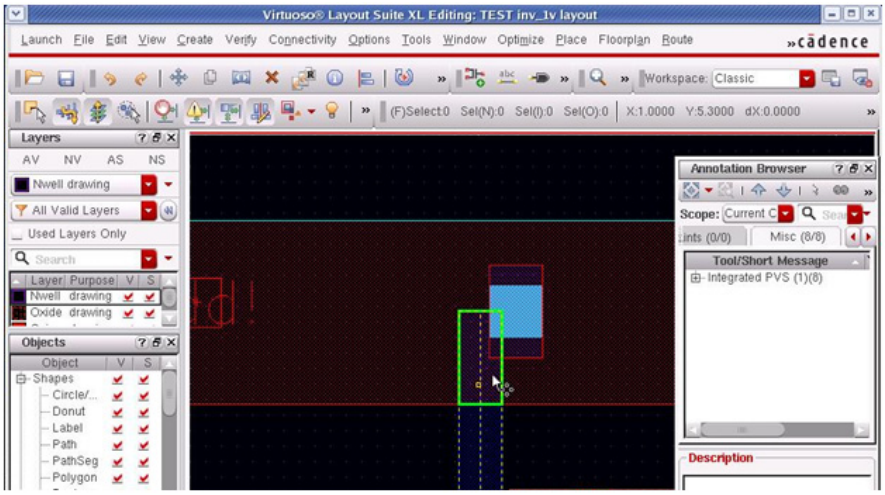

Figure 3: Virtuoso DRC technology

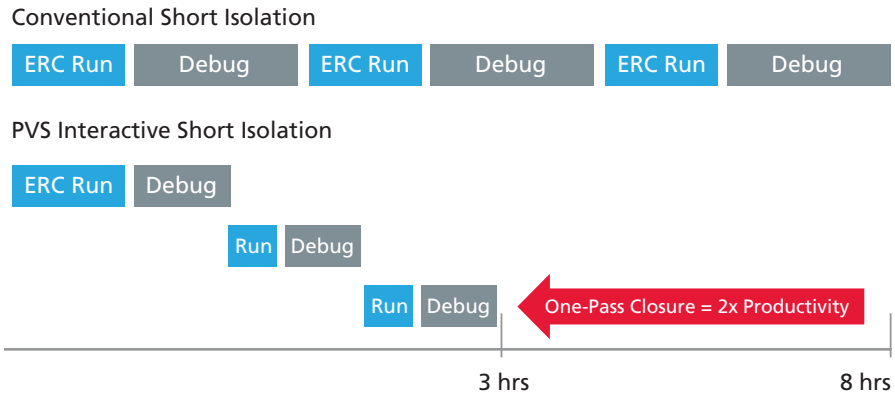

Figure 4: The Interactive Short Locator improves productivity by at least 2x

pre-layout stage. It can also be used to verify that third-party IP blocks satisfy the designer's reliability standards.

Constraint Validator

The PVS Constraint Validator shortens total turnaround time and improves design quality by detecting design errors in the very early stages of the IC development process, and by validating the design at the final stage. This new PVS tool is able to verify the correctness of created layout according to specified constraints. For example, whether all nets that should be routed symmetrically are indeed symmetrical, or whether halo distance is being taken into account. The Constraint Validator can detect errors in the implementation stage that conventional tools would only reveal during the very last parasitic extraction stage (i.e., symmetrical layout impacted by neighbor parasitic effect). The Constraint Validator is also used in the Cadence mixed-signal flow to ensure mixed-signal routing integration constraints are implemented correctly by the router.

Predictable debug cycle

Designers often spend more time on design rule checking (DRC) and layout versus schematic (LVS) debugging. The unpredictable debugging time can cause delays in schedule, leading to loss of product revenue. PVS provides two innovative debug solutions to help designers find and fix design issues in a foreseeable time period.

Interactive Short Locator

Shorts, especially power/ground shorts, are the most difficult debug issues. The PVS Interactive Short Locator facilitates one-pass short isolation to deliver an efficient and intuitive LVS debug solution that helps designers quickly detect and solve short issues. Designers can start debug analysis while the run is in progress, as soon as first results are available.

Graphical LVS debug

Identifying the causes of complex LVS mismatches is extremely time-consuming. The PVS Graphical LVS Debug solution accelerates identification of complex LVS mismatches in cell/block designs. By showing all errors and warnings in a consistent and simplified graphical view, users can easily debug complex LVS mismatches and identify differences between schematic and layout information. PVS also features the industry's first Verilog-compatible netlist-based LVS debug capability.

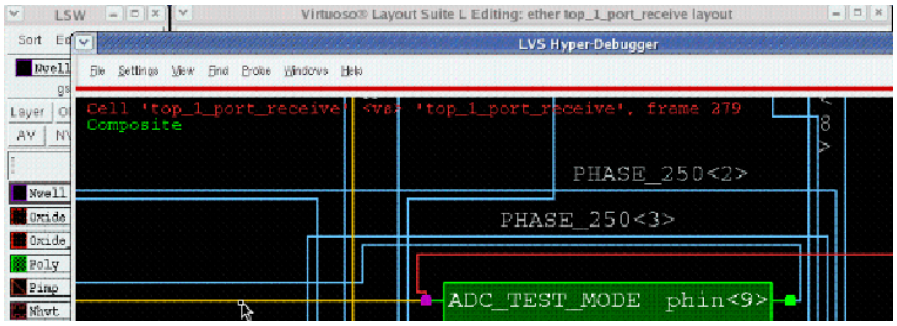

Figure 5: The Virtuoso GUI shows the graphical LVS debug environment

Error results visualization and management

The PVS Results Manager provides an easy-to-use, interactive error-navigation system to efficiently review, waive, and correct physical verification issues. The Results Manager can be launched within Virtuoso and Encounter environments. An interface with a high-performance, high-capacity design data viewer—Cadence QuickView—enables PVS users to efficiently debug extremely large system-on-chip (SoC) designs with design-file sizes in the tens-of-gigabytes range.

Competitive performance for design throughput

PVS delivers multi-processor performance that is highly competitive with other physical verification solutions. Large designs can also take advantage of the PVS distributed multi-threading processing architecture that leverages low-cost, off-the-shelf compute platforms to greatly accelerate design throughput.

Drop-in compatibility with industry-standard formats

All PVS rule files and output files are compatible with industry-standard formats. This allows PVS users to leverage their existing investments in rule decks and infrastructure with less effort for translation or scripts. Rule decks execute natively on PVS, and PVS reports design errors in an intuitive, predictable, and familiar way. This greatly accelerates tool and flow validation and integration.

QRC flow compatibility

PVS can accelerate the physical verification cycle time by streamlining the post-layout simulation flow. It supports Cadence QRC Extraction flows, and provides the TECHLIB set-up feature to make the PVS-to-QRC parasitic extraction flow easy to use. Both GUI and batch support are provided for SPICE, SPEF, DSPF, and extracted view outputs from QRC Extraction.

Signoff-ready, production-proven solution

PVS is production-proven, with hundreds of successful customer tapeouts in advanced nanometer process technologies from multiple foundries.

Cadence Services and Support

- Cadence application engineers can answer your technical questions by telephone, email, or Internet—they can also provide technical assistance and custom training
- Cadence certified instructors teach more than 70 courses and bring their real-world experience into the classroom
- More than 25 Internet Learning Series (iLS) online courses allow you the flexibility of training at your own computer via the Internet
- Cadence Online Support gives you 24x7 online access to a knowledgebase of the latest solutions, technical documentation, software downloads, and more

cadence®

Cadence is transforming the global electronics industry through a vision called EDA360. With an application-driven approach to design, our software, hardware, IP, and services help customers realize silicon, SoCs, and complete systems efficiently and profitably. **www.cadence.com**

22545 01/12 MK/DM/PDF