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AHB Verification IP

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Overview

The process of verification is getting complex with every passing year; this is due to the fact that complexities of chips are increasing. With such an increasing design complexity, verification tends to consume up to 60-80% project resources and often represents a bottleneck. Having all this in mind, SmartDV has developed number of Verification IP's, which has been created by verification engineers with decades of experience in verifying complex chips.

The SmartDV Verification IP (VIP) for AHB provides an efficient and simple way to verify the ARM AMBA AHB. The SmartDV VIP for AHB is fully compliant with ARM AMBA 3.0 AHB Specification and provides the following features:

- The model supports key features of ARM AMBA 3 AHB including burst transfers, spilt transactions, early burst termination and locked transfers.
- The model has a rich set of configuration parameters to control AHB functionality.

Features

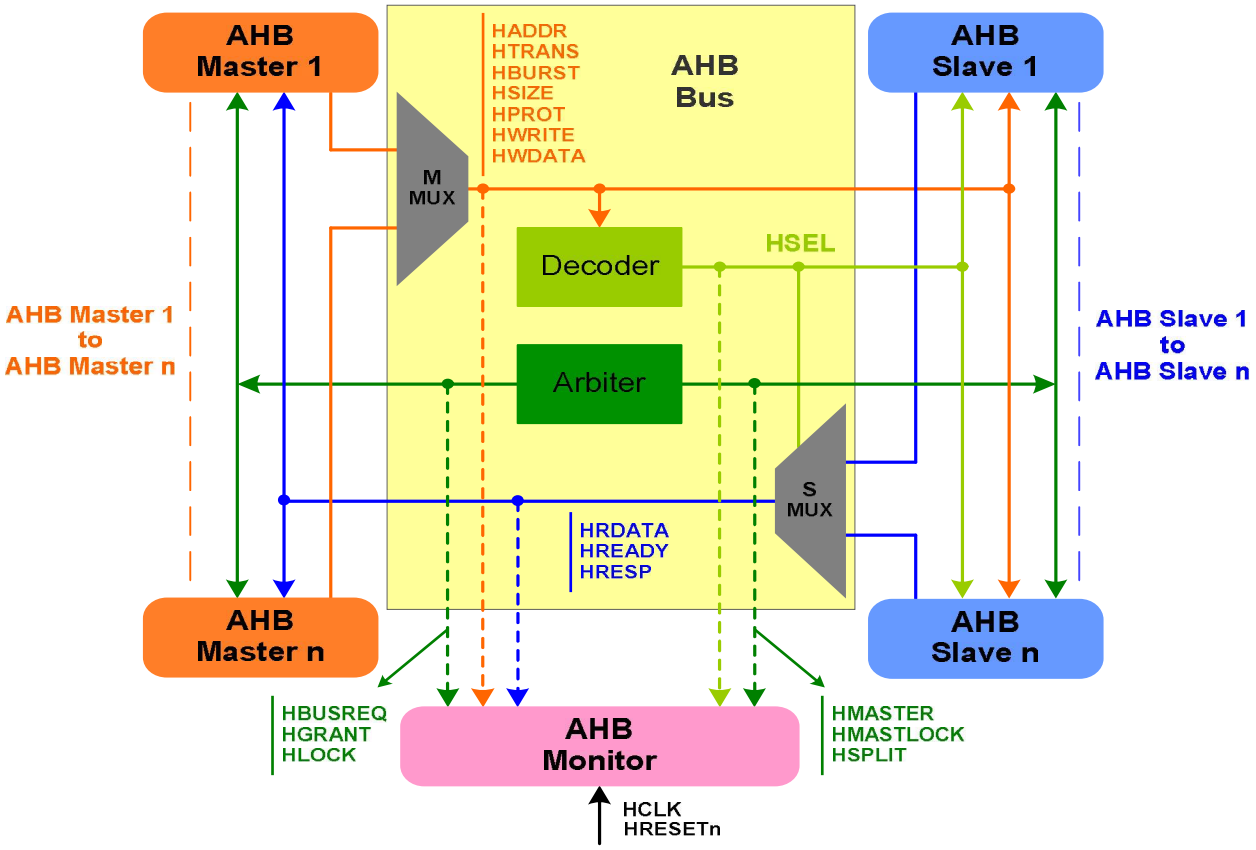
- Implemented in **Unencrypted OpenVera, Verilog, SystemC, SystemVerilog and Specman E.** .
- Supported RVM, AVM, **VMM**, OVM, UVM and non-standard verify env.
- Compliant with ARM AMBA 3 AHB specification.
- Supports ARM11 extension
- Supports both AHB and AHB Lite operation.
- Support AMBA AHB Master, AHB Slave, AHB Monitor and AHB Checker.
- Support for multiple slaves.
- Supports all ARM AMBA 3 AHB data and address widths
- Supports all protocol transfer types, burst transfers and response types.
- Support for all the transfer sizes.
- Supports constrained randomization of protocol attributes.
- Flexibility to send completely configured data.
- Slave supports fine grain control of response per address or per transaction.
- Master supports fine grain control of busy state insertion and master aborting.
- Supports Early burst termination and locked transfers.
- Supports split and retry transfers.
- Ability to inject errors during data transfer.
- Retry or cancel of a transfer on error.

- Support for programmable wait states.
- Supports FIFO memory.
- Rich set of configuration parameters to control AHB functionality.
- On-the-fly protocol and data checking.
- Notifies the testbench of significant events such as transactions, warnings, timing and protocol violations.
- Built in coverage analysis.
- Callbacks in master, slave and monitor for various events.
- Status counters for various events on bus.
- AHB Verification IP comes with complete testsuite to test every feature of AHB specification.

Benefits

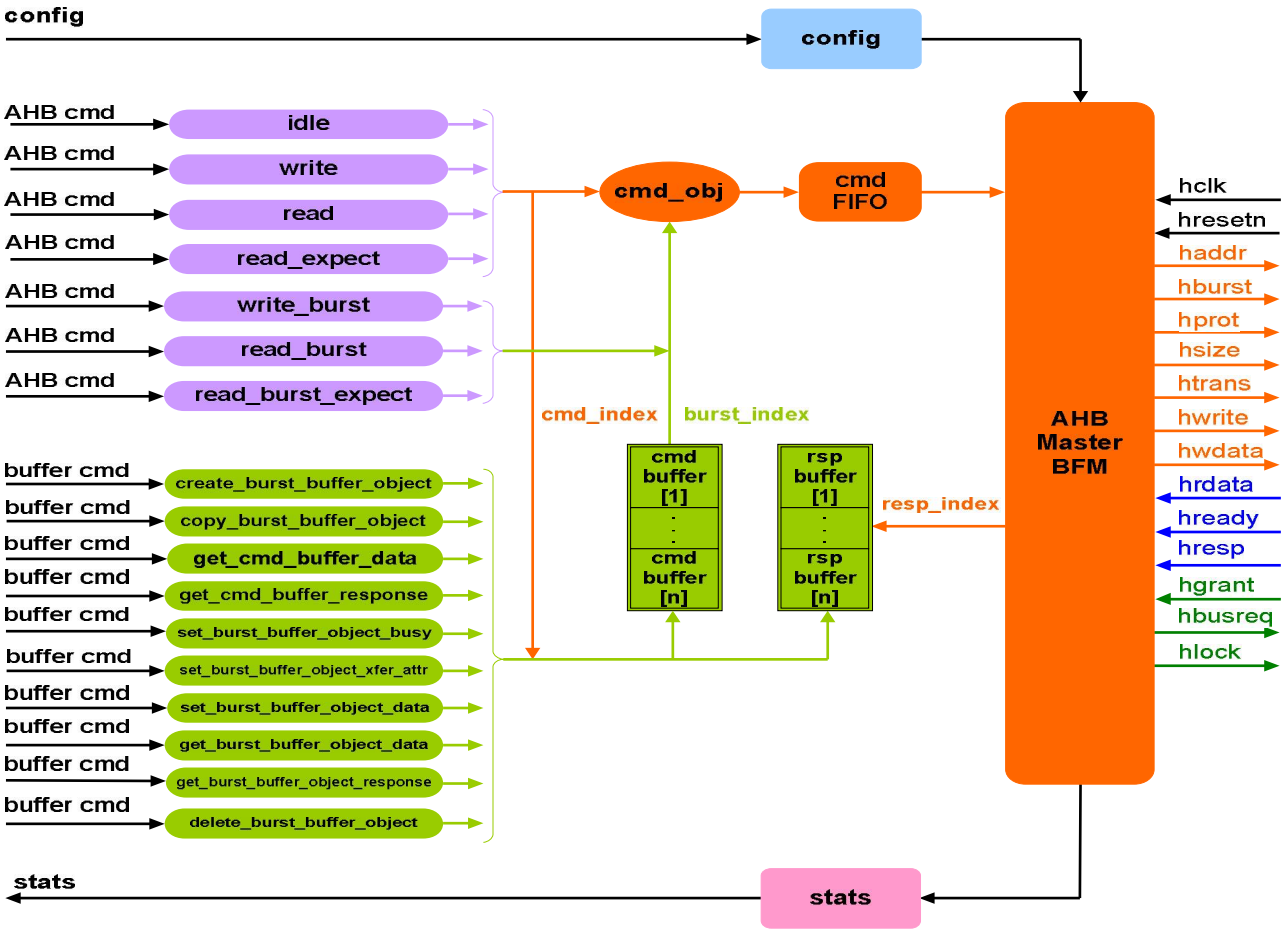
- Faster testbench development and more complete verification of AHB designs.
- Simplifies results analysis.
- Integrates easily into OpenVera, SystemVerilog, Specman E, SystemC, Verilog
- Runs in every major simulation environment

AHB Verification IP Topology


AHB Master 1
HADDR
HTRANS
HBURST
HSIZE
HPROT
HWRITE
HWDATA
AHB Bus
AHB Slave 1
M MUX
Decoder
HSEL
AHB Master 1 to AHB Master n
Arbiter
AHB Slave 1 to AHB Slave n
S MUX
HRDATA
HREADY
HRESP
AHB Master n
AHB Slave n
HBUSREQ
HGRANT
HLOCK
AHB Monitor
HMASTER
HMASTLOCK
HSPLIT
HCLK
HRESETn

Master Behavior

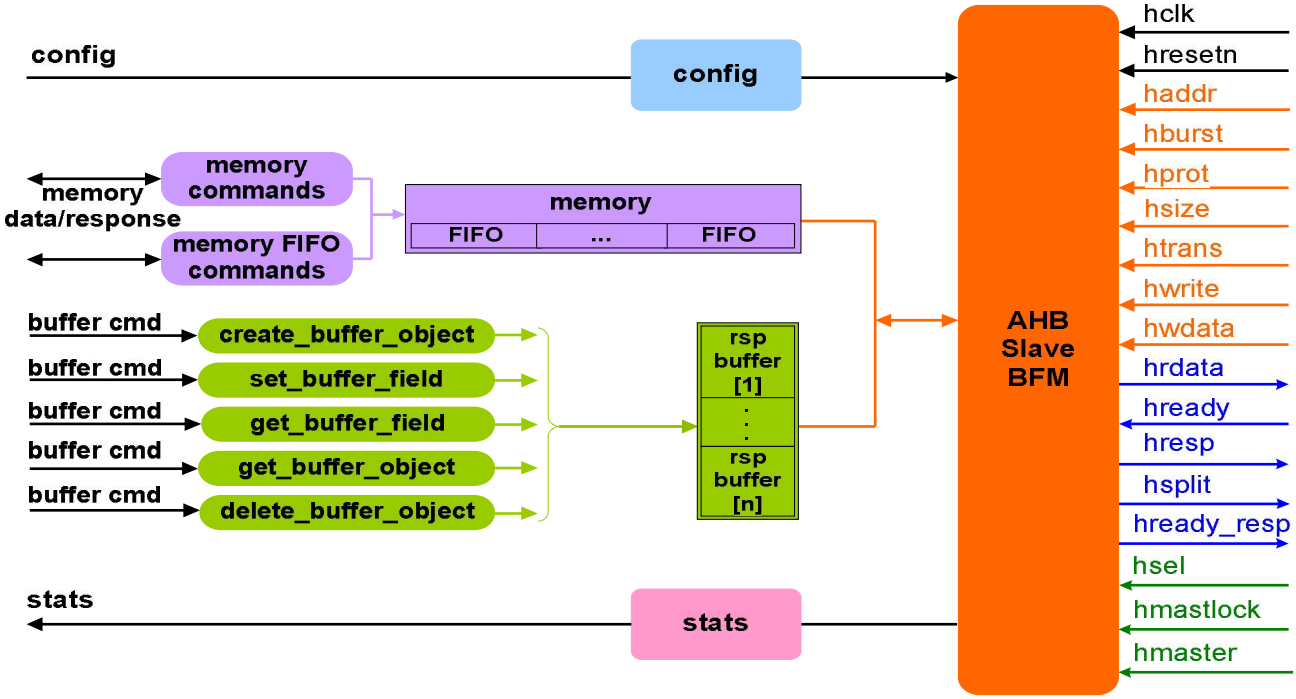
AHB master is first configured with different configuration parameters. The master then initiates requests based on read and write commands from the testbench. These commands include low level commands and burst commands. For burst commands, a new command buffer is created and the burst transfer attributes are set using rich set of buffer commands. Read data and response from slave are stored in response buffer. User can access this buffer to get read data or slave response. Error injection is supported by forcing the Master to abort the transfer at the specified position. Master BFM supports user callbacks for read and write command processing. The results of a transfer can be obtained from the response buffer using buffer commands.



Slave Behavior

Each slave is first configured with different configuration parameters. A slave device monitors the bus to determine if it has been selected for a transfer request. It will always respond to a transfer request if it has been selected. The slave responds to read requests by sending data which can be fed through internal memory model. For write requests, the slave receives data transmitted by the master and passes it to the internal memory model. Each memory location can be configured to respond with different response. Memory space can be configured to

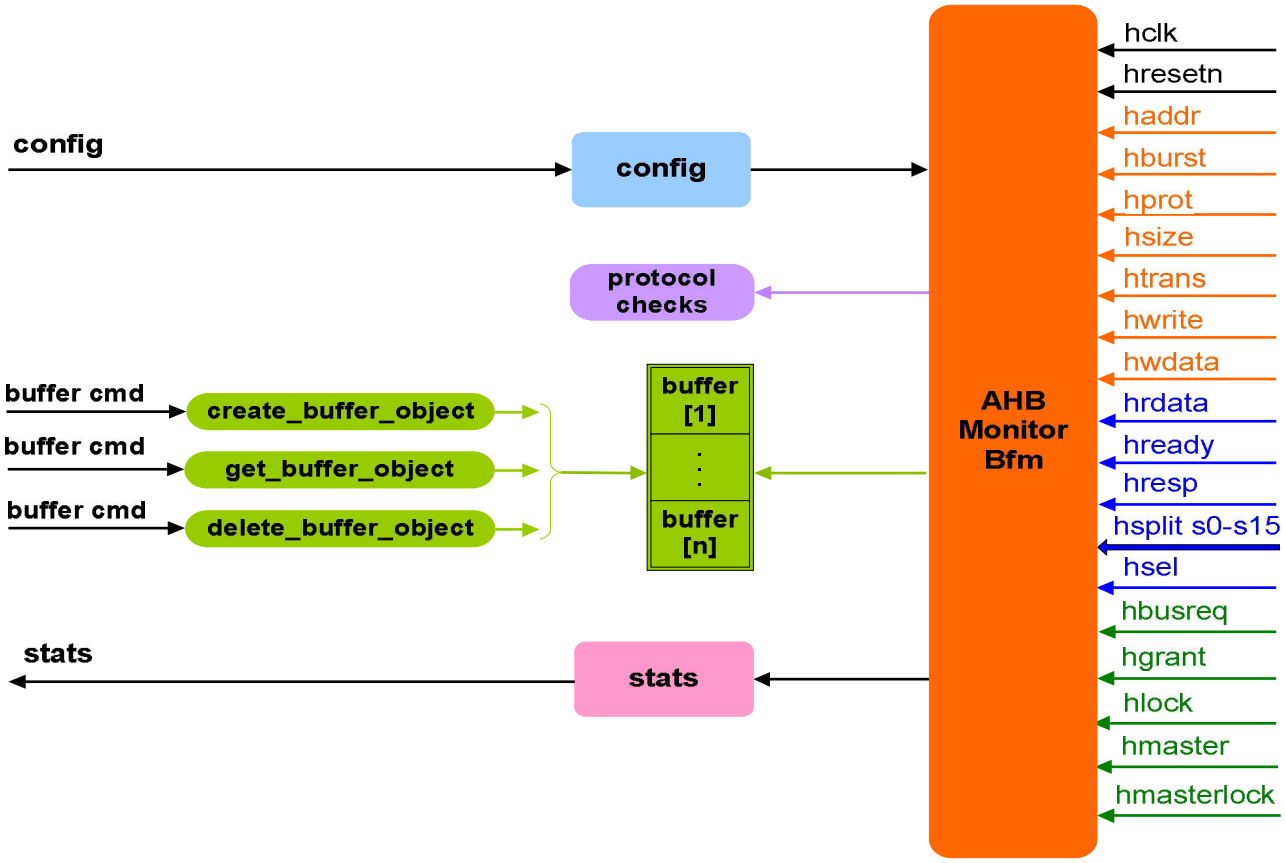
provide FIFO memory. The slave can be made to act erroneously by forcing it to respond with inserting wait states, errors, retry, split response to transfer requests. Slave's response to a transfer can be controlled using buffers as well, by creating response buffers and setting response attributes in it using rich set of buffer commands. Slave BFM supports user callbacks for read and write response processing.



Monitor Behavior

Monitor is first configured with different configuration parameters. A monitor monitors the bus for protocol errors and timing errors. Monitor also keeps track of all the accesses on bus and these stats can be accessed any time during simulation.

Transfer request and response attributes are stored in a buffer which can be obtained using rich set of buffer commands. The Monitor also logs all transactions into a file that can be configured through the use of methods.



Supported Simulators

- VCS
- NC-SIM
- Modelsim
- Questasim

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