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APB Verification IP

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Overview

The process of verification is getting complex with every passing year; this is due to the fact that complexities of chips are increasing. With such an increasing design complexity, verification tends to consume up to 60-80% project resources and often represents a bottleneck. Having all this in mind, SmartDV has developed number of Verification IP's, which has been created by verification engineers with decades of experience in verifying complex chips.

The SmartDV Verification IP (VIP) for APB provides an efficient and simple way to verify the AMBA APB. The SmartDV VIP for APB is fully compliant with AMBA APB 3.0/4.0 Specification and provides the following features:

The model supports key features of ARM AMBA APB 3.0/4.0 including write transfers, read transfers and error response.

- The model has a rich set of configuration parameters to control APB functionality.

Features

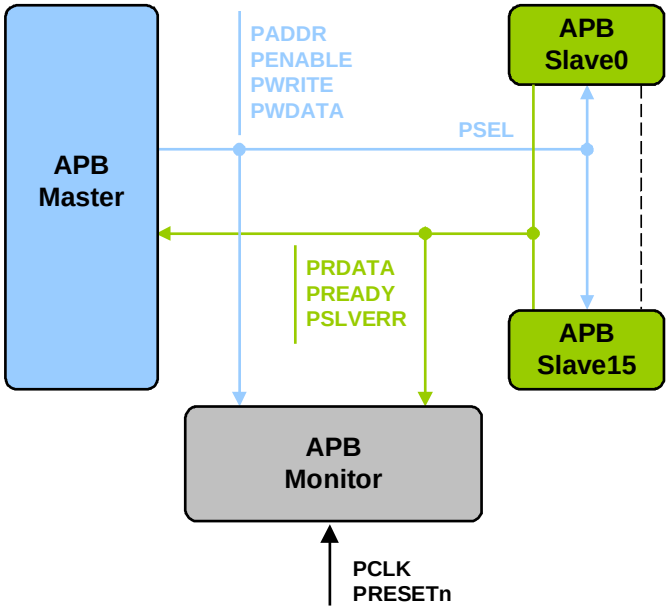
- Implemented in **Unencrypted OpenVera, Verilog, SystemVerilog, SystemC, Specman E.**
- Supported RVM, AVM, VMM, OVM, UVM and non-standard verify env.
- Compliant to ARM AMBA APB 3.0/4.0 protocol
- Support AMBA APB Master, APB Slave, APB Monitor and APB Checker.
- Support for multiple slaves
- Supports all ARM AMBA APB 3.0/4.0 data and address widths.
- APB4 support protected accesses
  - Normal/Privileged
  - Secure/Non-secure
  - Data/Instruction
- APB4 support for write strobe signal to enable sparse data transfer on the write data bus.
- Supports different command types
  - IDLE
  - WRITE
  - READ
  - READ_EXPECT
- Supports constrained randomization of protocol attributes.

- Supports unaligned address accesses
- Flexibility to send completely configured data.
- Slave supports fine grain control of response per address or per transfer.
- Random PSLVERR insertion.
- Programmable Wait state insertion.
- Programmable Timeout insertion.
- Programmable number of idle cycles
- Ability to inject errors during data transfer.
- Supports FIFO memory.
- Rich set of configuration parameters to control APB functionality.
- On-the-fly protocol and data checking.
- Notifies the testbench of significant events such as transactions, warnings, timing and protocol violations.
- Built in coverage analysis.
- Callbacks in master, slave and monitor for various events.
- Status counters for various events on bus.
- APB Verification IP comes with complete testsuite to test every feature of ARM AMBA APB 3.0/4.0 specification

Benefits

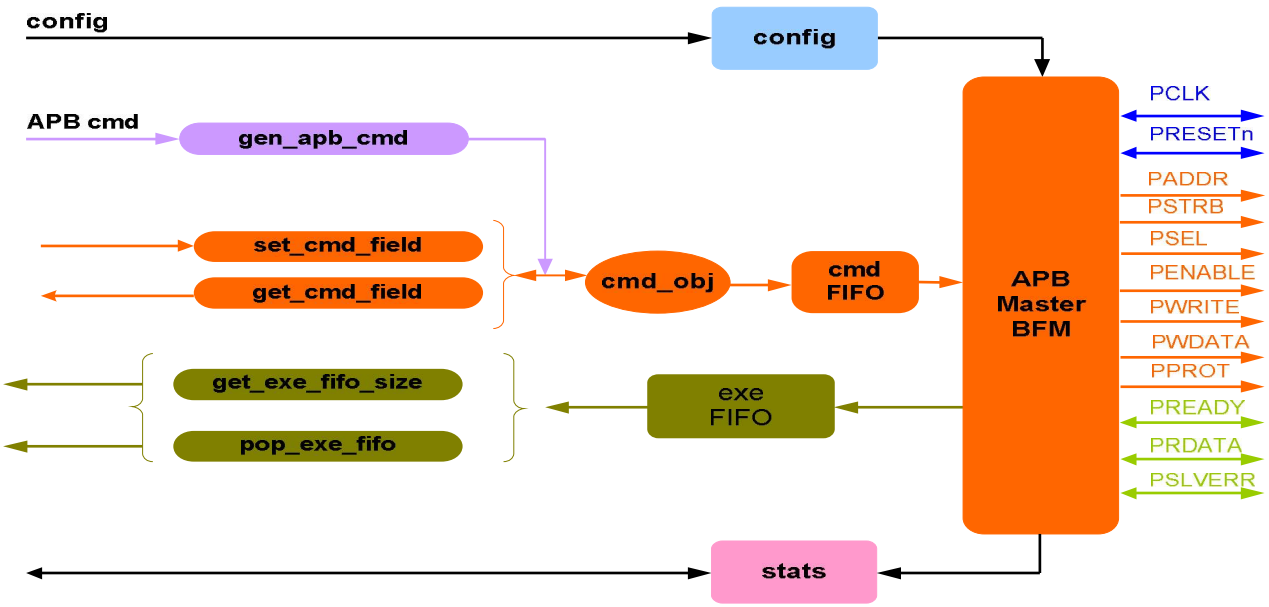
- Faster testbench development and more complete verification of APB 3.0/4.0 designs.
- Compliant to ARM AMBA APB 3.0/4.0 protocol
- Easy to use command interface simplifies testbench control and configuration of master and slave.
- Simplifies results analysis.
- Integrates easily into OpenVera, SystemVerilog, Verilog.
- Runs in every major simulation environment.
- Written in 100% SystemVerilog and VMM. So runs faster and easy to use with VMM testbenches.

APB Verification IP Topology



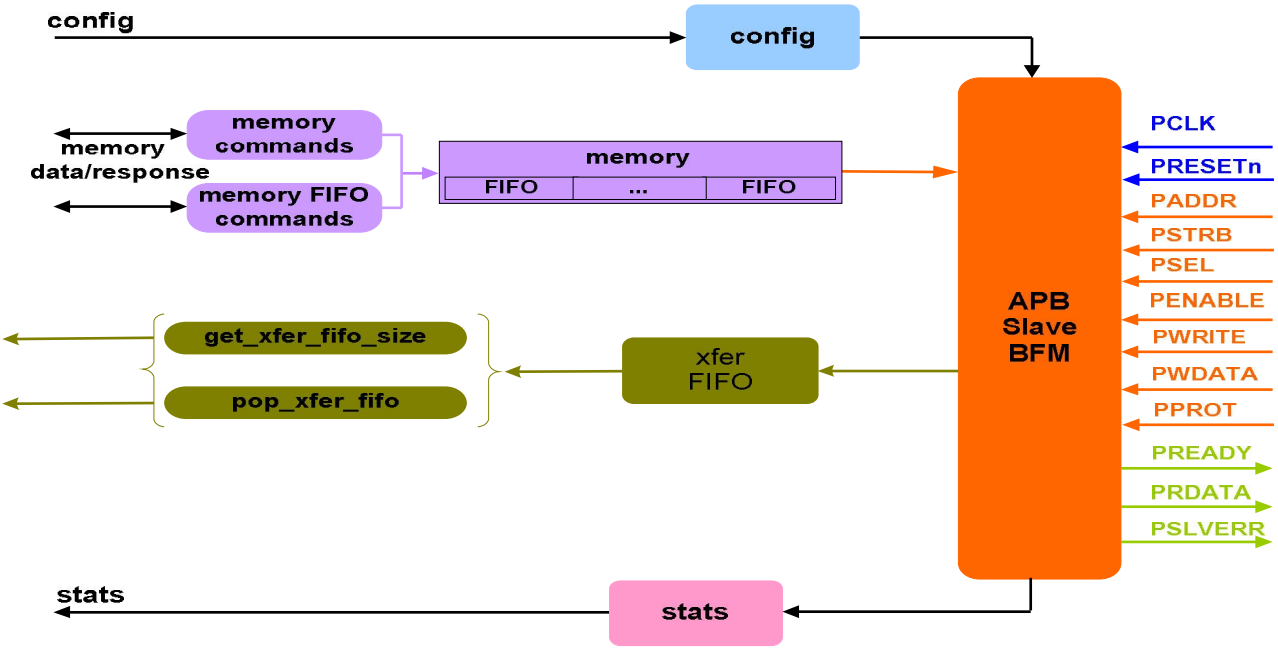
Master Behavior

APB master is first configured with different configuration parameters. SmartDV's AMBA APB verification IP supports rich set of configuration parameters to control each and every possible functionality. This is stored in config object in above block diagram. User is provided with rich set of methods to generate different types of transfers. The master then initiates requests based on write, read , read expect and idle commands from the testbench. Read data and response from slave are stored in exe FIFO. User can access this FIFO to get read data or slave response. Master BFM supports user callbacks for read and write command processing. User can override the default behavior of the Master BFM using these callbacks. At the end of execution of methods, status counters are updated. User can access this counters anytime during simulation. Master BFM can also be configured to log all the access into a log file, with different debug levels. This can be later used for post processing.



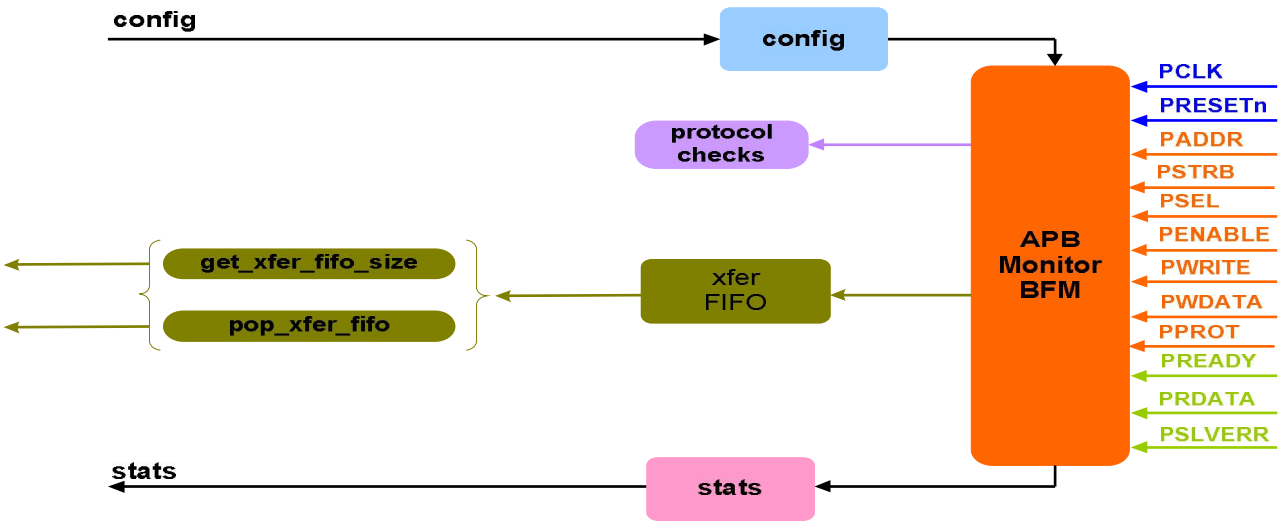
Slave Behavior

Each slave is first configured with different configuration parameters. A slave device monitors the bus to determine if it has been selected for a transfer request. It will always respond to a transfer request if it has been selected. The slave responds to read requests by sending data that can be fed through internal memory model. For write requests, the slave receives data transmitted by the master and passes it to the internal memory model. Each memory location can be configured to respond with different response. Memory space can be configured to provide FIFO memory. Transfer request and response attributes are stored in transfer FIFO. The slave can be made to act erroneously by forcing it to respond with timeout or assert PSLVERR to transfer requests. Slave BFM supports user callbacks for read and write response processing. User can override the default behavior of the Slave BFM using these callbacks. At the end of execution of methods, status counters are updated. User can access this counters anytime during simulation. The Slave also logs all transactions into a file that can be configured through the use of methods.



Monitor Behavior

Monitor is first configured with different configuration parameters. A monitor monitors the bus for protocol errors and timing errors. Monitor also keeps track of all the accesses on bus and these stats can be accessed any time during simulation. Transfer request and response attributes are stored in transfer FIFO. The Monitor also logs all transactions into a file that can be configured through the use of methods. Monitor implements functional coverage.



Supported Simulators

- VCS
- NC-SIM
- Modelsim
- Questasim

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