SmartDV Technologies India Private Limited
14/B, 2nd Cross, SR Layout,
Bangalore, India: 560017
E-Mail: info@smart-dv.com
http://www.smart-dv.com

ARINC 429 Verification IP

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Overview

The process of verification is getting complex with every passing year; this is due to the fact that complexities of chips are increasing. With such an increasing design complexity, verification tends to consume up to 60-80% project resources and often represents a bottleneck. Having all this in mind, SmartDV has developed number of Verification IP's, which has been created by verification engineers with decades of experience in verifying complex chips.

The SmartDV Verification IP (VIP) for ARINC 429 provides an efficient and simple way to verify the ARINC 429. The SmartDV VIP for ARINC 429 is fully compliant with ARINC SPECIFICATION 429 PART 1-17 provides the following features:

- The model has a rich set of configuration parameters to control ARINC 429 functionality.
- Ability to detect and insert various types of error.
- The source is capable of inserting various transmit errors.
- The sink is capable of detecting various received errors.

Features

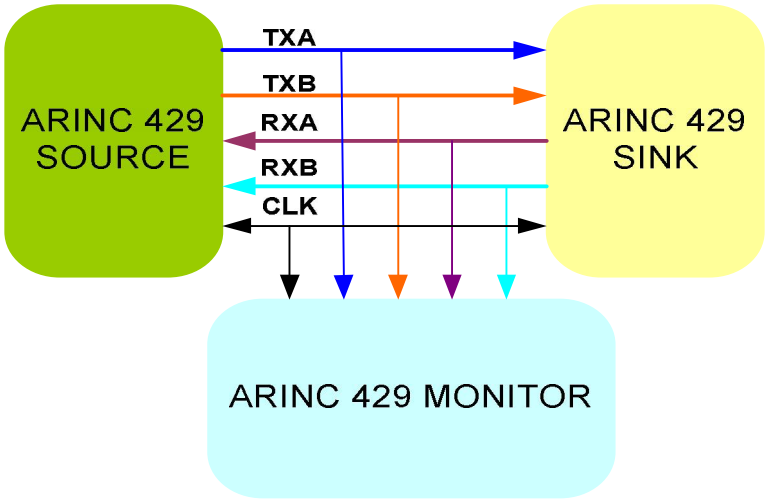
- Implemented in **Unencrypted OpenVera, SystemVerilog, Verilog, SystemC and Specman E.**
- Supported RVM, AVM, VMM, OVM, UVM and non-standard verify env.
- Compliant with ARINC SPECIFICATION 429 PART 1-17.
- Supports 32 bit words containing a 24 bit data portion containing the actual information, and an 8 bit label describing the data itself.
- Supports Transmission rates at either a low speed – 12.5 kHz – or a high speed – 100kHz.
- Supports two speeds for data transmission
  - Low speed operation 12.5 kHz, with an actual allowable range of 12 to 14.5 kHz.
  - High speed operation is 100 kHz ± 1% allowed.
- Supports bipolar and Return-to-Zero encoding format.
- Supports following data types
  - Binary – BNR – Transmitted in fractional two's complement notation
  - Binary Coded Decimal – BCD – Numerical subset of ISO Alphabet No. 5
  - Discrete Data – Combination of BNR, BCD or individual bit representation
  - Maintenance Data and Acknowledgement – Requires two-way communication

  - Williamsburg/Buckhorn Protocol – A bit-oriented protocol for file transfers
- Supports duplex or two-way communication in Maintenance Data and Acknowledgement between source and sink.
- Glitch injection and detection
- Supports all types of errors insertion/detection as given below:
  - Missing SOT word
  - LDU Sequence Number Error
  - Parity Errors
  - Word Count Errors
  - CRC Errors
  - Time Out Errors
- Notifies the test bench of significant events such as transactions, warnings, and protocol violations.
- Status counters for various events.
- Callbacks in source and sink for various events.
- Built in functional coverage analysis.
- ARINC 429 Verification IP comes with **complete test suite** to verify each and every feature of ARINC 429 specification.

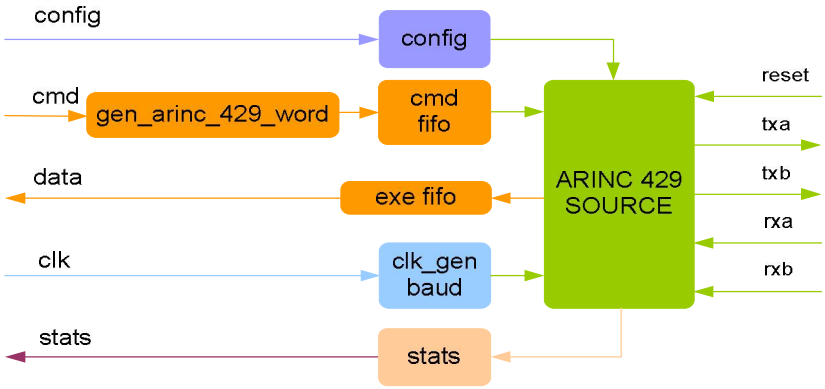
Benefits

- Faster test bench development and more complete verification of ARINC 429 designs.
- Easy to use command interface simplifies test bench control and configuration of Source and Sink.
- Integrates easily into **OpenVera, SystemVerilog, Verilog, Specman, SystemC.**
- Simplifies results analysis.
- Runs in every major simulation environment

ARINC 429 Verification IP Topology



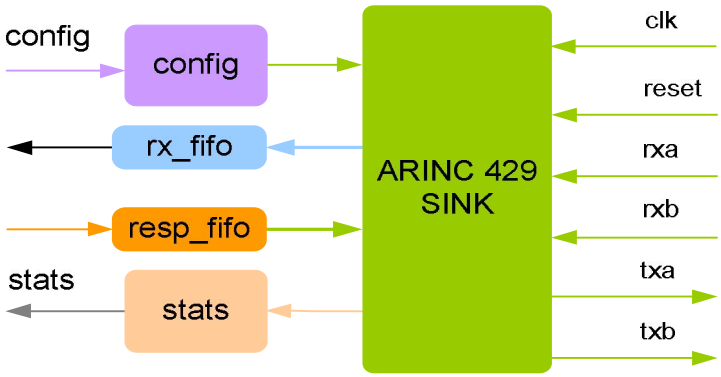
ARINC 429 source BFM Behavior



ARINC 429 verification IP acts as a Source. Source is first configured with different configuration parameters. Configuration parameters are baud rate, transmit FIFO depth. Error insertion can be performed for common serial data and word transmission errors. FIFO's are used to store data transmitted.

At each stage of transmission, callbacks are executed for giving control to user to processing the data being transmitted. Status counters are updated at the end of transmission.

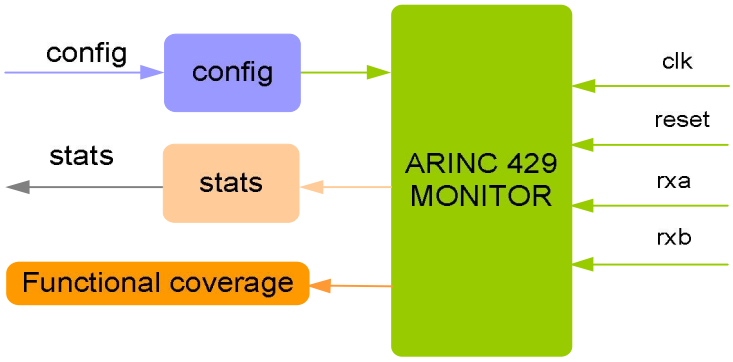
ARINC 429 sink BFM Behavior



ARINC 429 verification IP acts as a sink. Sink is first configured with different configuration parameters. Configuration parameters are baud rate, receive FIFO depth. Sink recovers the clock from serial data, and samples the words. Error detections is performed for common serial data and word transmission errors. FIFO's are used to store data received during serial.

At each stage of reception, callbacks are executed for giving control to user to processing the data being transmitted. Status counters are updated at the end of transmission.

Monitor Behavior



Monitor is first configured with different configuration parameters. A monitor monitors the ARINC 429 bus, recovers the clock, and samples words. Monitor also keeps track of all the access on bus and these stats can be accessed any time during simulation. Protocol checking begins after a valid reset, or without a reset if configured for this condition. The Monitor also logs all transactions into a file that can be configured through the use of log methods.

Supported Simulators

- VCS
- NC-SIM
- Modelsim
- Questasim

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