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AXI Verification IP

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Overview

The process of verification is getting complex with every passing year; this is due to the fact that complexities of chips are increasing. With such an increasing design complexity, verification tends to consume up to 60-80% project resources and often represents a bottleneck. Having all this in mind, SmartDV has developed number of Verification IP's, which has been created by verification engineers with decades of experience in verifying complex chips.

The SmartDV Verification IP (VIP) for AXI provides an efficient and simple way to verify the ARM AMBA AXI. The SmartDV VIP for AXI is fully compliant with ARM AMBA 3/4 AXI Specification and provides the following features:

- The model supports key features of ARM AMBA 3/4 AXI including separate address/control and data phases, ability to issue multiple outstanding transactions, out-of-order transaction completion, write and read data interleaving, separate read and write data channels, burst-based transactions with only start address issued and support for unaligned data transfers using byte strobes.
- It has a rich set of configuration parameters to control AXI functionality.
- It supports configurable transactions, exclusive access, unaligned data transfers, configurable slave response and FIFO memory.

Features

- Implemented in **Unencrypted OpenVera, Verilog, Specman E, SystemC and SystemVerilog**.
- Supported RVM, AVM, **VMM**, OVM, **UVM** and non-standard verify env.
- Compliant with the latest ARM AMBA AXI 3.0/4.0 specification.
- Supports AXI Master, AXI Slave, AXI Monitor and AXI Checker.
- Supports all ARM AMBA AXI 3.0/4.0 data and address widths.
- Supports all protocol transfer types, burst types, burst lengths and response types.
- Supports constrained randomization of protocol attributes.
    - Separate address/control and data phases. Separate read and write data channels.
- Support for burst-based transactions with only start address issued.
- Unaligned data transfers using byte strobes.
- Ability to issue multiple outstanding transactions.

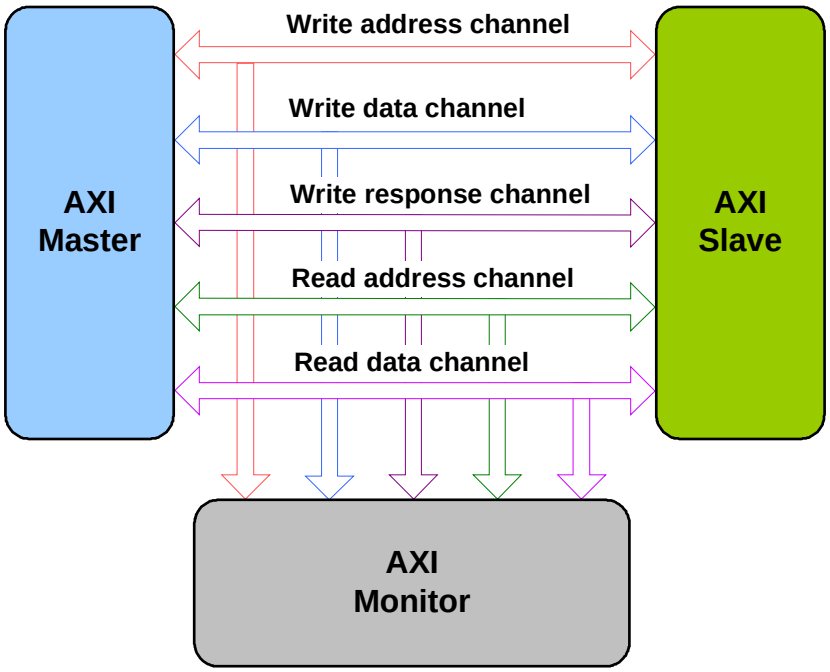
- Out of order transaction completion support.
- Write data and read data interleaving support.
- Atomic access support
    - Exclusive
    - Locked response
- Configurable write and read interleave depth.
- AXI4 support
    - Longer bursts up to 256 beats
    - Quality of Service
    - Multiple region interface
- AXI4 Lite support
    - Data bus width of 32-bit or 64-bit
    - Burst lenght of 1
- AXI4-Stream support.
- Multiple data streams
    - Byte stream
    - Continuous aligned stream
    - Continuous unaligned stream
    - Sparse stream
- Byte types
    - Data byte
    - Position byte
    - Null byte
- Support for transfer interleaving and ordering processes.
- Slave supports fine grain control of response per address or per transaction.
- Configurable wait states on different channels.
- Supports FIFO memory.
- Supports functionality to verify ACE and CCI interconnect functionality for cache.
- Protected accesses
    - Normal/Privileged
    - Secure/Non-secure
    - Data/Instruction
- Rich set of configuration parameters to control AXI functionality.
- On-the-fly protocol and data checking.
- Notifies the testbench of significant events such as transactions, warnings, timing and protocol violations.
- Built in coverage analysis.
- Callbacks in master, slave and monitor for various events.
- Status counters for various events on bus.
- AXI Verification IP comes with complete testsuite to test every feature of ARM AMBA AXI 3.0/4.0 specification.

Benefits

- Faster testbench development and more complete verification of AXI designs.
- Simplifies results analysis.

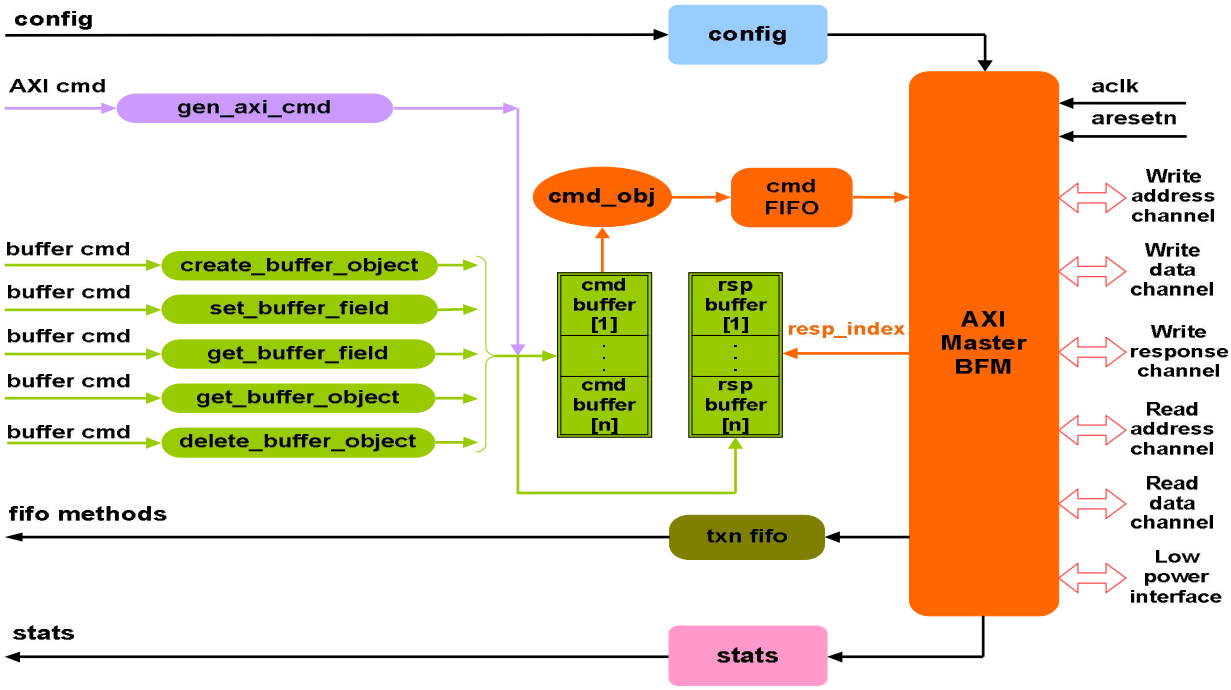
- Integrates easily into **OpenVera, SystemVerilog, Verilog, SystemC, Specman E.**
- Runs in every major simulation environment.

AXI Verification IP Topology



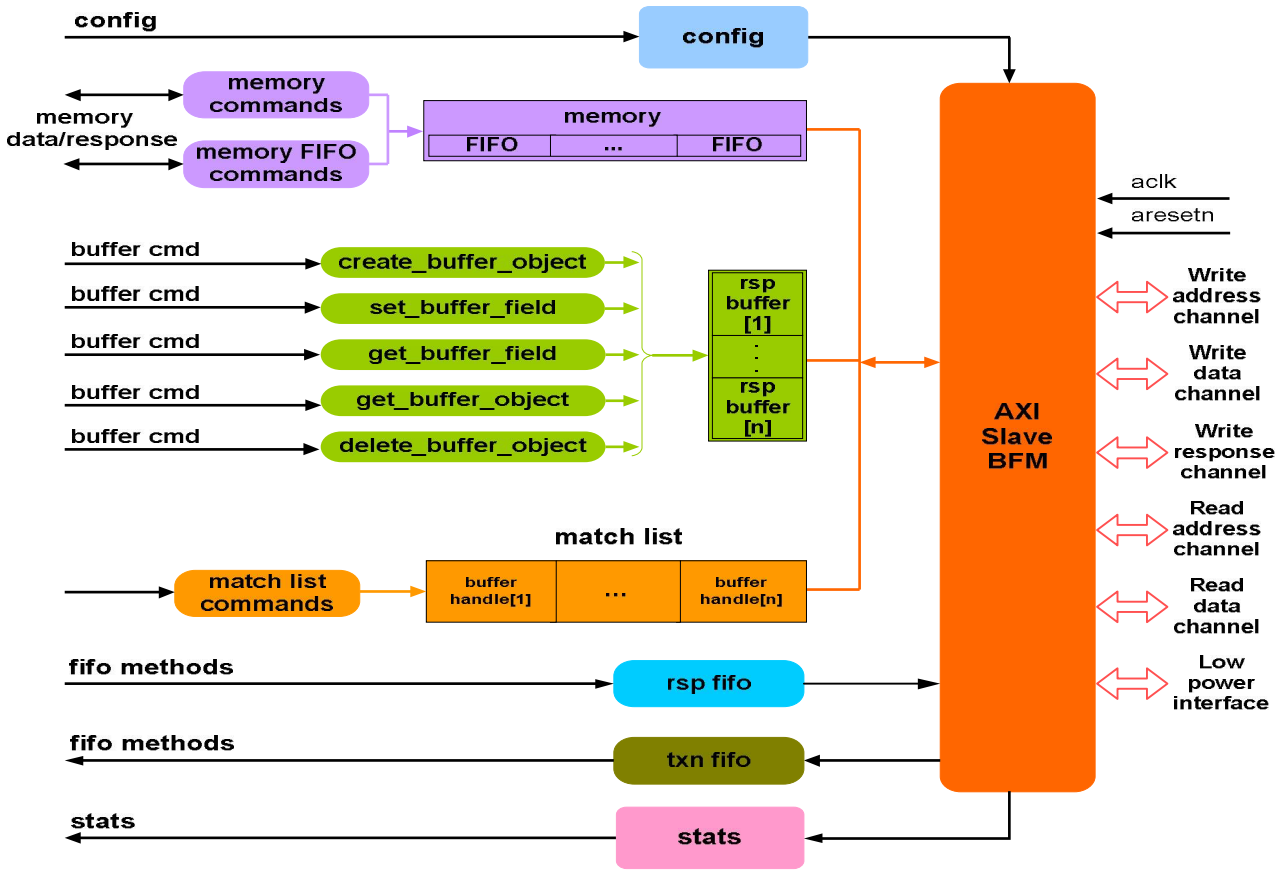
Master Behavior

AXI master is first configured with different configuration parameters. SmartDV's AXI verification IP supports rich set of configuration parameters to control each and every possible functionality. This is stored in config object in above block diagram. User is provided with rich set of methods to generate different types of transfers. A command buffer is created for a transaction and transaction attributes are set in it using rich set of buffer commands. Once the transaction is issued, Master initiates the appropriate transfer after reading attributes from the transaction buffer. The results of a transaction can be obtained from the response buffer using rich set of buffer commands. Other than the response buffer, transfer and response attributes are also saved in transaction FIFO. Master supports user callbacks for AXI command processing. User can override the default behavior of the Master using these callbacks. At the end of execution of methods, status counters are updated. User can access these counters anytime during simulation. Master can also be configured to log all the access into a log file, with different debug levels. This can be later used for post processing.



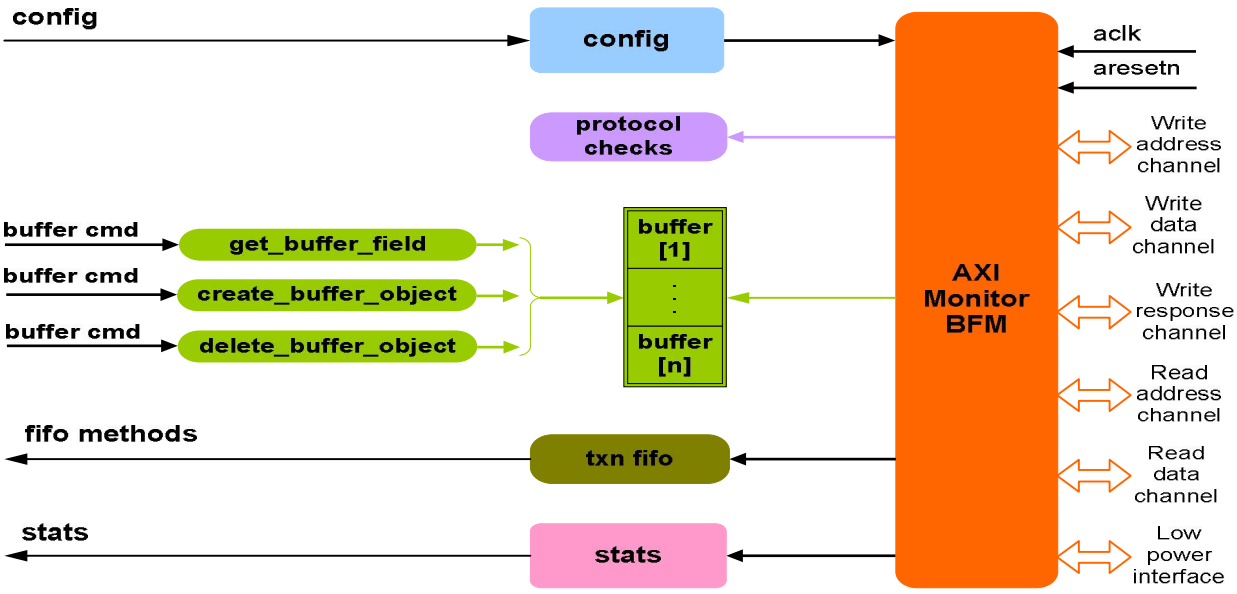
Slave Behavior

AXI slave is first configured with different configuration parameters. Slave monitors the bus for a valid transaction. For write requests, Slave receives data transmitted by Master and writes into the internal memory model. Slave responds to read requests by sending data from the internal memory model. Memory space can be configured to provide FIFO memory. Slave's response to a transaction can be controlled by creating response buffers and setting response attributes in it using rich set of buffer commands. The response buffer is set to recognize the signature of the transaction and is added to the match list. On detection of a valid transaction, the Slave scans through the match list to get the response buffer matching the transaction signature. Once the signature matches, the Slave responds w.r.t the response attributes in the response buffer. Transfer request and response attributes are stored in transaction FIFO. Slave supports user callbacks for read and write response processing. User can override the default behavior of the Slave using these callbacks. At the end of execution of methods, status counters are updated. User can access these counters anytime during simulation. The Slave also logs all transactions into a file that can be configured through the use of methods.



Monitor Behavior

Monitor is first configured with different configuration parameters. A monitor monitors the bus for protocol errors and timing errors. The protocol checks include channel handshake ordering. Monitor also keeps track of all the accesses on bus and these stats can be accessed any time during simulation. Protocol checking begins after a valid reset, or without a reset if configured for this condition. Transfer request and response attributes are stored in a buffer, which can be obtained using rich set of buffer commands and in a transaction FIFO, which can be accessed using rich set of FIFO commands. The Monitor also logs all transactions into a file that can be configured through the use of methods. Monitor supports user callbacks for accessing transaction on the bus.



Supported Simulators

- VCS
- NC-SIM
- Modelsim
- Questasim

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