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MIPI-BIF Verification IP

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Overview

The process of verification is getting complex with every passing year; this is due to the fact that complexities of chips are increasing. With such an increasing design complexity, verification tends to consume up to 60-80% project resources and often represents a bottleneck. Having all this in mind, SmartDV has developed number of Verification IP's, which has been created by verification engineers with decades of experience in verifying complex chips.

The SmartDV Verification IP (VIP) for MIPI-BIF provides an efficient and simple way to verify the MIPI-BIF single-wire communication Interface. The SmartDV VIP for MIPI-BIF is fully compliant with version 1.00 of the MIPI-BIF Bus Specification and provides the following features:

- The model supports the key features of MIPI-BIF version 1.00.
- The model has a rich set of configuration parameters to control MIPI-BIF functionality.
- Ability to detect and insert various types of error.

Features

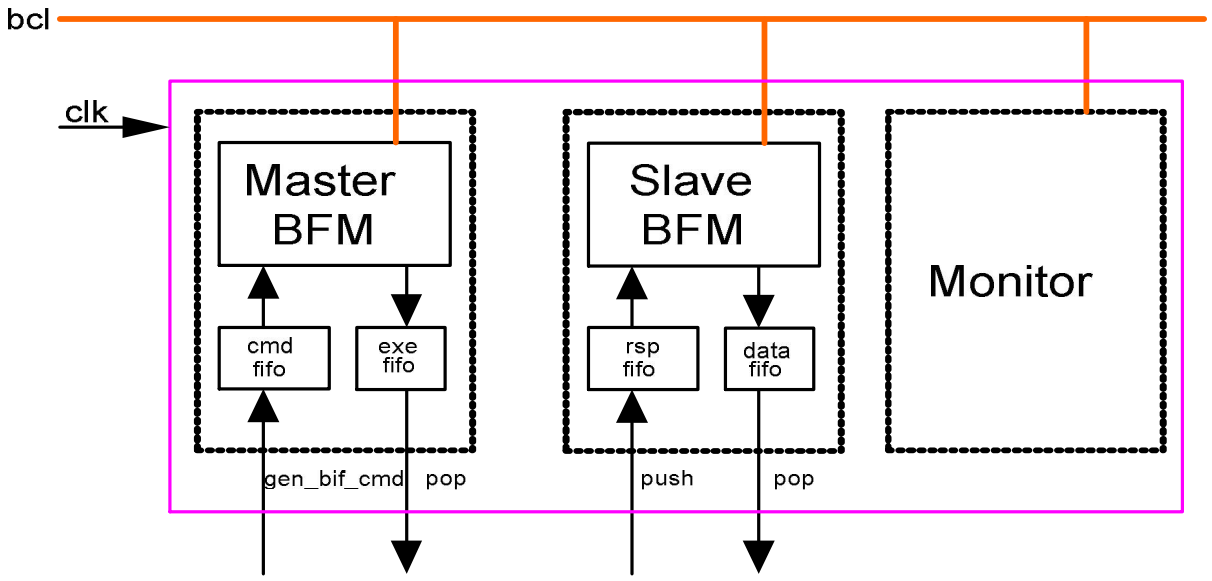
- Implemented in **Unencrypted OpenVera, Verilog, SystemC and SystemVerilog**.
- Supported RVM, AVM, **VMM**, OVM, UVM and non-standard verify env.
- Supports version 1.00 MIPI BIF Specification.
- Single wire, open drain communication interface.
- Single Master and Multi-Slaves (up to 256 slaves).
- Supports Broadcast, Multicast and Unicast words.
- Supports various power modes.
- Supports all types of Bus commands.
- Supports UID procedure.
- Supports various kinds of errors generation and detection on BIF
    - General Communication Error.
    - Parity Error.
    - Inversion Error.
    - Invalid Word Length.
    - Timing Error.
    - Unknown Bus Command.
    - Wrong Command Sequence.
    - Bus Collision.

    - Slave Busy.
    - Slave Fatal Error.
- Interrupt capability supported.
- Supports the DDB Level 1 and Level 2 data structures.
- Supports various kinds of functions,
    - Protocol function.
    - Slave control function.
    - NVM function.
    - Temperature sensor function.
    - Authentication function.
- Glitch insertion and detection.
- Monitor, Detects and notifies the test bench of all protocol and timing errors.
- Supports constraints Randomization.
- Status counters for various events in bus.
- Callbacks in master and slave for various events.
- MIPI BIF Verification IP comes with complete test suite to test every feature of MIPI BIF specification.
- Functional coverage for complete MIPI BIF features.

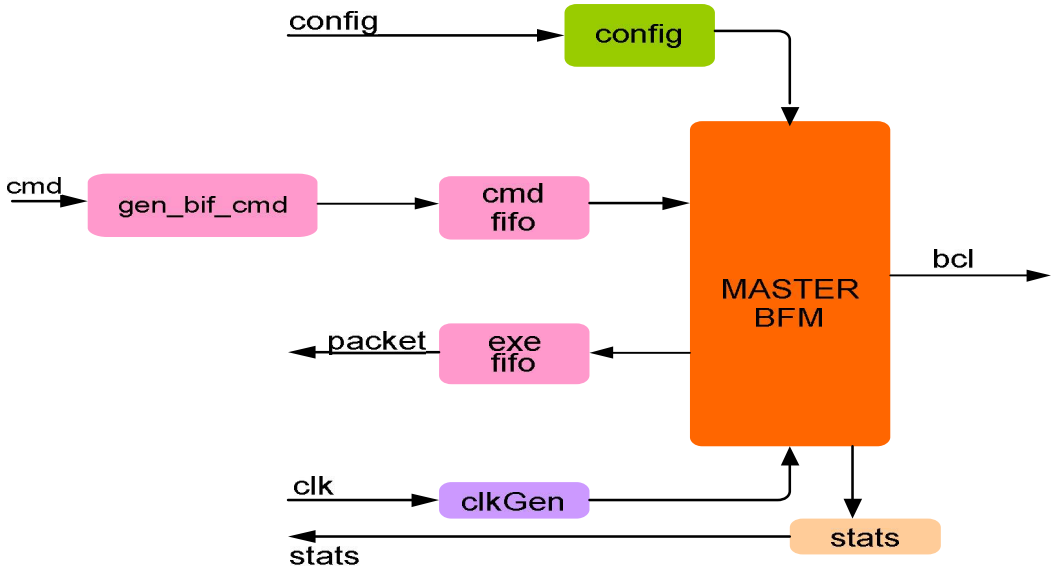
Benefits

- Faster testbench development and more complete verification of MIPI-BIF designs.
- Simplifies results analysis.
- Integrates easily into **OpenVera, SystemVerilog, Verilog, Specman, SystemC.**
- Runs in every major simulation environment

MIPI-BIF Verification IP Topology



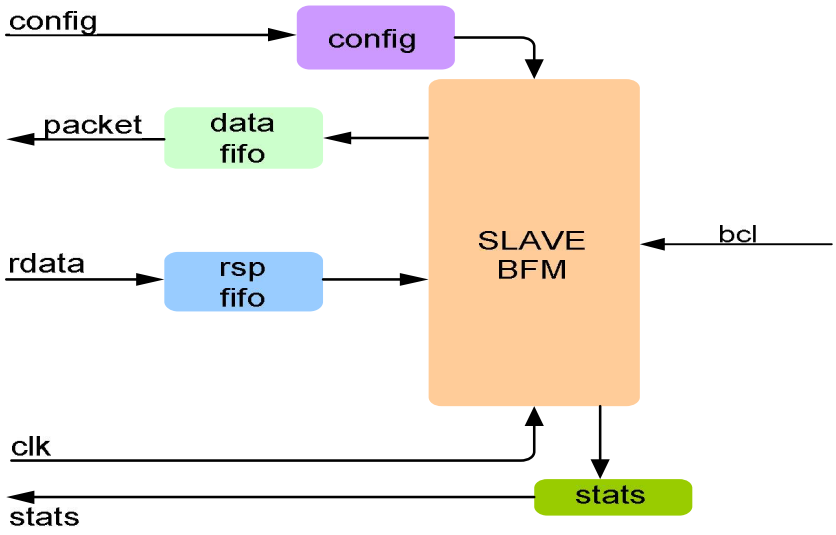
Master Behavior



MIPI-BIF VIP Master is first configured with different configuration parameters. Configuration parameters are baud rate, transmit FIFO depth. The Master initiates the transmission via BCL (Bus Communication Line) based on the types of bus commands from the test cases. Master supports Broadcast, Multicast and Unicast words. Master supports to injection of various errors and timing violations. At the end of transmitting each word transmission stats are updated.

At each stage of transmission, callbacks are executed for giving control to user to processing the data being transmitted.

Slave Behavior

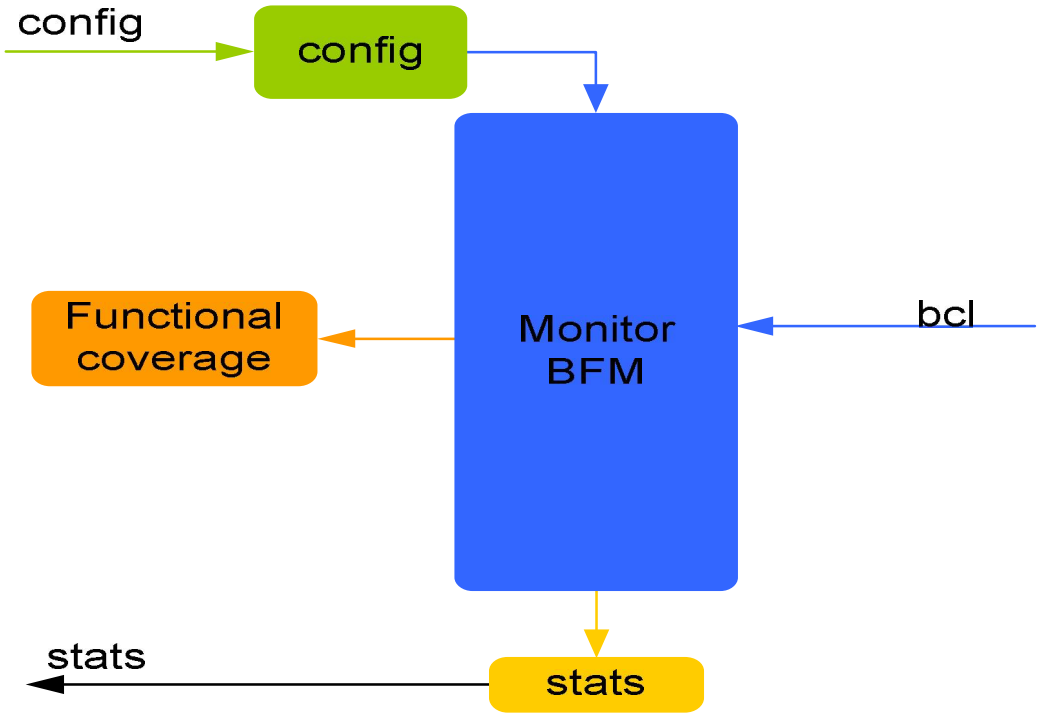


Each slave is first configured with different configuration parameters. Configuration parameters are baud rate, receive FIFO depth. Slave receives the commands via BCL (Bus Communication Line) and takes the appropriate actions based on the received bus commands. For write transaction, the slave receives the data transmitted by the master and passes it to the data FIFO. For read transaction, the slave responds to read requests by sending read data which can be provide through its response FIFO. Slave supports various kinds of functions.

At each stage of reception, callbacks are executed for giving control to user to processing the data being transmitted. Status counters are updated at the end of transmission.

Monitor Behavior

Monitor is first configured with different configuration parameters. A monitor monitors the MIPI-BIF bus for protocol errors and timing errors. Monitor also keeps track of all the access on bus and these stats can be accessed any time during simulation. The Monitor also logs all transactions into a file that can be configured through the use of methods. Monitor implements the functional coverage, which user can modify to add more coverage in object oriented way.



Supported Simulators

- VCS
- NC-Sim
- Modelsim
- Questasim

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