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MIPI CSI2 Verification IP

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Overview

The process of verification is getting complex with every passing year; this is due to the fact that complexities of chips are increasing. With such an increasing design complexity, verification tends to consume up to 60-80% project resources and often represents a bottleneck. Having all this in mind, SmartDV has developed number of Verification IP's, which has been created by verification engineers with decades of experience in verifying complex chips.

The SmartDV Verification IP (VIP) for MIPI CSI2 provides an efficient and simple way to verify the MIPI CSI2 protocol bus. The SmartDV VIP for MIPI CSI2 is fully compliant with version 1.0 of the MIPI CSI2 Bus Specification and provides the following features:

Features

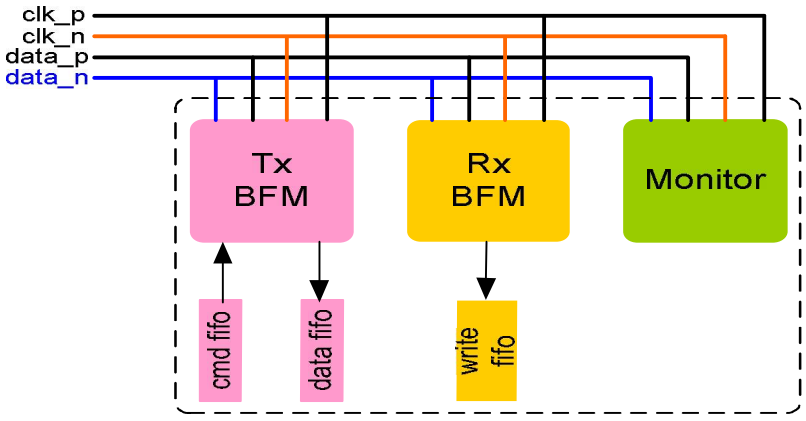
- Implemented in **Unencrypted OpenVera, SystemVerilog, Verilog, SystemC and Specman E.**
- Supported RVM, AVM, VMM, OVM, UVM and non-standard verify env.
- Full MIPI CSI2 Tx/Rx functionality.
- Supports forward escape ULPM on all Data Lanes.
- Supports image applications with varying pixel formats from six to twenty-four bits per pixels.
- Supports short and long packets.
- Supports all types of short packets.
- Supports all types of long packets.
- Supports all lane configurations.
- Supports all virtual channel identifier.
- Supports various methods to interleave the transmission of different image data formats
    - Interleaved data transmission using data type value
    - Interleaved data transmission using virtual channels
- Supports various methods to interleave the data transmission using data type value
    - Packet level interleaved data transmission
    - Frame level interleaved data transmission
- Supports differential mode of operation.
- Supports various kind of Tx and Rx errors generation and detection
    - SoT error
    - Sync error

    - Word count error
    - Sync length error
    - Checksum error
    - ECC error
- Monitor detects and notifies the testbench of all protocol and timing errors.
- Supports constraints Randomization.
- Supports PHY-Protocol Interface(PPI).
- Status counters for various events in bus.
- Callbacks in node transmitter, receiver and monitor for user processing of data.
- MIPI CSI-2 Verification IP comes with complete test suite to test every feature of MIPI CSI-2 specification.
- Functional coverage for complete MIPI CSI-2 features
- Control bus is supported by means of I2C

Benefits

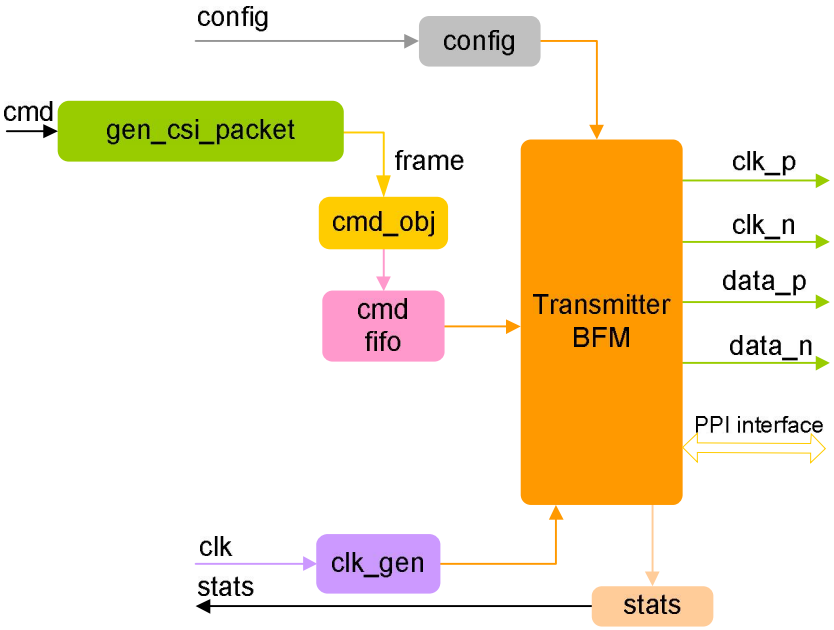
- Faster testbench development and more complete verification of MIPI CSI designs.
- Simplifies results analysis.
- Integrates easily into **OpenVera, SytemVerilog, Verilog, Specman E, and SystemC**
- Runs in every major simulation environment

MIPI CSI2 Verification IP Topology



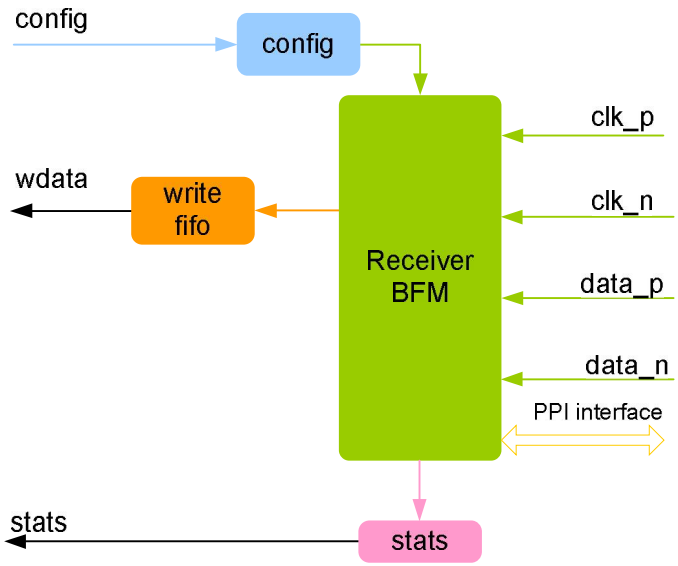
Transmitter Behavior

MIPI CSI2 Tx is first configured with different configuration parameters. MIPI CSI2 BFM initiates the possible frames based on the various MIPI CSI2 commands from the testbench. User uses the rich set of methods for sending frames on Tx path of BFM. At each stage of sending frame, callbacks are executed for giving control to user to processing the frame. Status counters are updated at the end of transmission of frame.



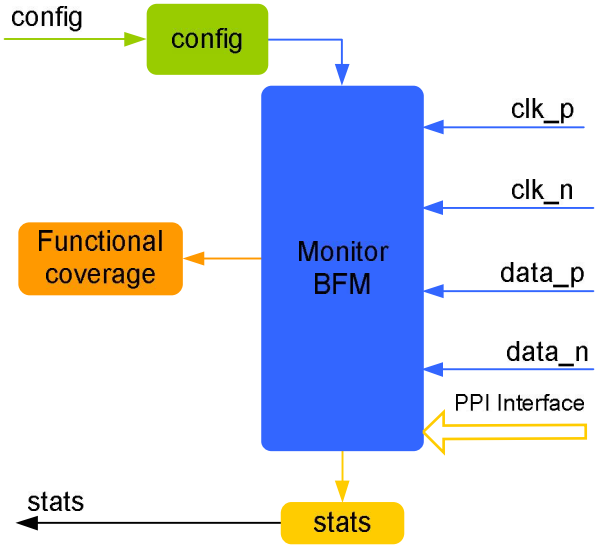
Receiver Behavior

MIPI CSI2 Receiver is first configured with different configuration parameters. A Receiver device monitors the bus to determine the data transaction. At each stage of frame collections, callbacks are used for give control to the user to process the frame. At the end of frame reception, status counters are updated.



Monitor Behavior

Monitor is first configured with different configuration parameters. A monitor monitors the MIPI CSI2 bus for protocol errors and timing errors. Monitor also keeps track of all the accesses on bus, updates the status counters. These statuses can be accessed any time during simulation. Monitor also implemented the functional coverage points which user can extend to add or remove new functional coverage points.



Supported Simulators

- VCS
- NC-SIM
- ModelSim
- Questasim

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