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DDR2 Monitor Verification IP

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Overview

The process of verification is getting complex with every passing year; this is due to the fact that complexity of chips are increasing. With such an increasing design complexity, verification tends to consume up to 60-80% project resources and often represents a bottleneck. Having all this in mind, SmartDV has developed number of Verification IP's, which has been created by verification engineers with decades of experience in verifying complex chips.

The SmartDV Verification IP (VIP) for DDR2 Monitor provides an efficient and simple way to monitor the DDR2 traffic and collect data on bus. The SmartDV VIP for DDR2 Monitor is fully compliant with DDR2 Standard of JESD79-2C:

- Supports all the speeds and most of the vendors in market.
- Operates as a DDR2 protocol checker, Monitor and data collector

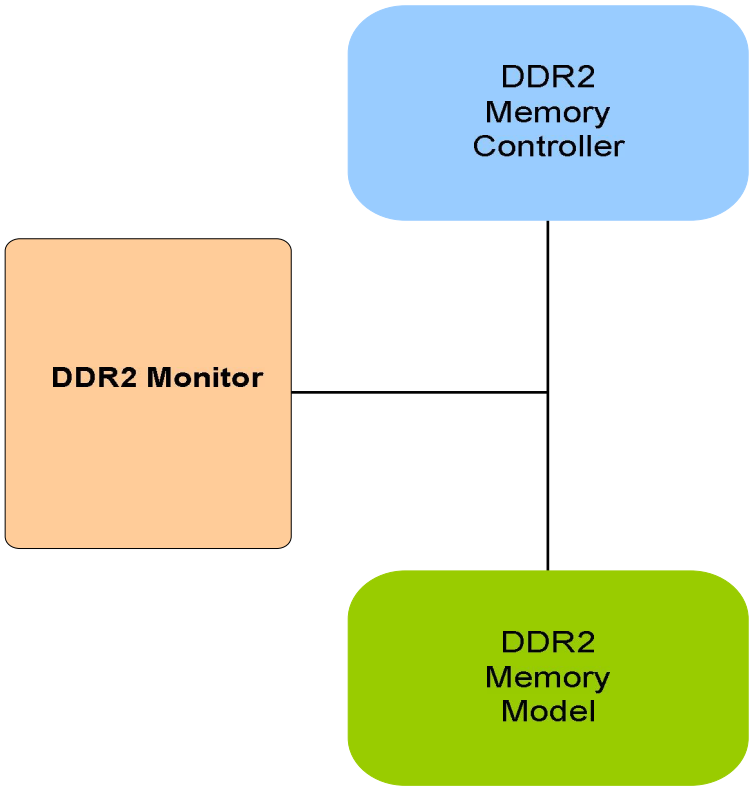
Features

- Implemented in **Unencrypted OpenVera, Verilog, SystemC and SystemVerilog**.
- Supported RVM, AVM, **VMM**, OVM, UVM and non-standard verify env.
- Supports 100% of DDR2 protocol.
- Supports all the DDR2 commands as per the specs.
- Supports programmable clock frequency of operation.
- Support all types of timing and protocol violation detection.
- Checks for following
  - Check-points include Initialization rules,
  - State based rules, Active Command rules,
  - Read/Write Command rules etc.
- Supports callbacks for user to get command data on bus.
- Bus-accurate timing for min, max and typical values.
- Notifies the testbench of significant events such as transactions, warnings, timing and protocol violations.

Benefits

- Faster testbench development and more complete verification of DDR2 designs.
- Simplifies results analysis.
- Integrates easily into OpenVera, SystemVerilog, SystemC, Verilog
- Runs in every major simulation environment
- Written in 100% SystemVerilog and VMM. So runs faster and easy to use with VMM testbenches.

DDR2 Monitor Verification IP Topology



Monitor Behavior

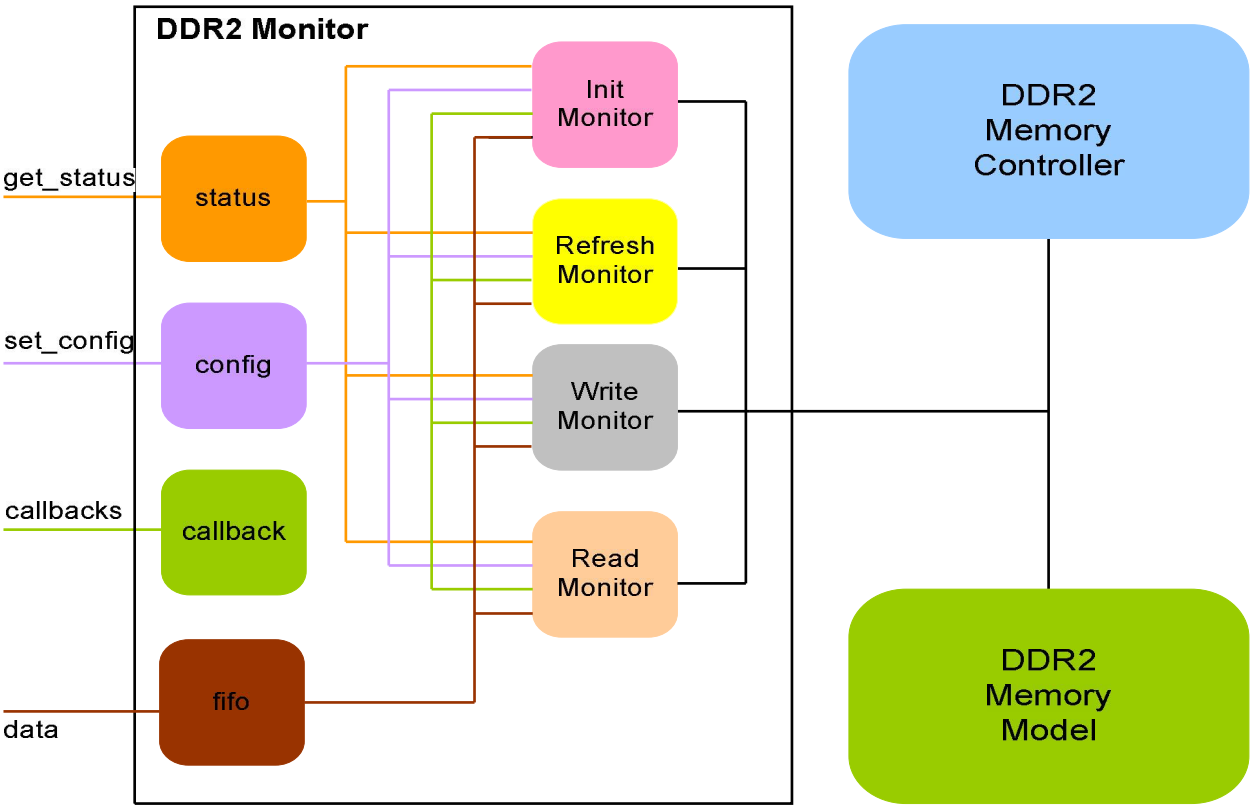
Monitor is first configured with different configuration parameters. This is stored in config object in above block diagram. After a valid reset and power up sequence (This can be skipped), All other sub monitors in DDR2 monitor become active. Whenever a valid access is detected, monitor collects complete command and data associated with command and executed the callback. Also status counters are updated to reflect the current status of the access.

A monitor monitors the DDR2 bus for protocol errors and timing errors. Monitor also keeps track of all the access on bus, and these stats can be accessed any time during simulation.

DDR2 monitor verification IP can also be configured to log all the access into a log file, with

different debug levels. This can be later used for post processing.

Monitor implements the functional coverage.



Supported Simulators

- VCS
- NC-Sim
- ModelSim

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