Smart DV Technologies India Private Limited
14/B, 2nd Cross, SR Layout,
Bangalore, India : 560017
E-Mail : info@smart-dv.com
http://www.smart-dv.com

Display Port Verification IP

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Overview

The process of verification is getting complex with every passing year; this is due to the fact that complexities of chips are increasing. With such an increasing design complexity, verification tends to consume up to 60-80% project resources and often represents a bottleneck. Having all this in mind, SmartDV has developed number of Verification IP's, which has been created by verification engineers with decades of experience in verifying complex chips.

The SmartDV Verification IP (VIP) for Display port provides an efficient and simple way to verify the Display port protocol bus. The SmartDV VIP for Display port is fully compliant with Display Port 1.2 specification and provides the following features:

- Supports Display Port source device and sink device.
- Supports both the Aux and Main link
- Support ECC

Features

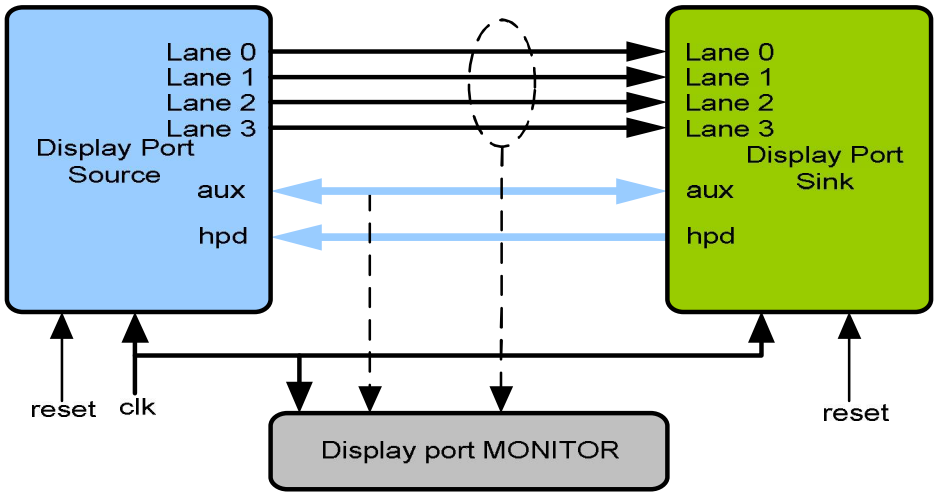
- Implemented in **Unencrypted OpenVera, SystemVerilog, Verilog, SystemC and Specman E.**
- Supported RVM, AVM, VMM, OVM, UVM and non-standard verify env.
- Full Display port source device and sink device functionality.
- Supports multi lanes upto 4 lanes.
- Supports control symbols for framing (Both Default & Enhanced framing mode).
- Supports serial & parallel bit ordering.
- Supports Interlaced & non-interlaced video stream.
- Supports Nibble interleaving (ECC).
- Supports main link, Aux link and Hot plug functionality.
- Supports ANSI8B10B encoding / decoding.
- Supports Serialization and de-serialization.
- Supports packing of all the video formats supported by the display port
- Supports packing of all secondary(audio) formats supported by the display port
- Supports HPD based link training.
- Supports inter lane skew insertion in source mode
- Supports de-skew in sink device mode
- Supports scrambler as in Display port specification
- Scrambler can enabled or disabled dynamically.

- Supports scrambler reset after every 512th symbols.
- Support on the fly generation of data.
- Detects and reports the following errors.
    - Invalid control character
    - Invalid data character
    - Invalid 10bit code
    - Sync errors
    - Scrambler errors
    - Single and multi-bit ECC errors
    - Invalid packing injection and detection
- Monitors, detects and notifies the test bench of significant events such as transactions, warnings, timing and protocol violations.
- Status counters for various events on bus.
- Callbacks in node transmitter, receiver and monitor for user processing of data.
- Display port Verification IP comes with **complete testsuite** to test every feature of Display port version 1.2 specifications.
- Functional coverage for complete Display port features.

Benefits

- Faster testbench development and more complete verification of Display port designs.
- Simplifies results analysis.
- Easy to use command interface simplifies testbench control and configuration of transmitter and receiver.
- Runs in every major simulation environment.

Display Port Verification IP Topology



Display Port Source Behavior

DP Source is first configured with different configuration parameters. DP BFM initiates the possible requests based on the various DP commands from the testbench. User uses the rich set of methods for sending frames (lines) on transmit path of BFM. Source device BFM packs the frames based on format and number of lanes, scrambles, encodes 8b/10b and drives serial data onto the serial lanes. At each stage of sending frame, callbacks are executed for giving control to user to processing the frame. Status counters are updated at the end of transmission of frame.

Display Port Sink Behavior

DP Sink device is first configured with different configuration parameters. A sink device, first tries to recover the clock, lock to correct 10 bit, decodes 10b to 8b, descrambles the data. Unpacks the data into frames (lines) and pushes into receive FIFO's. At each stage of frame/lines collections, callbacks are used for give control to the user to process the frame. At the end of frame reception, status counters are updated.

Monitor Behavior

Monitor is first configured with different configuration parameters. A monitor monitors the DP bus for protocol errors and timing errors. Monitor also keeps track of all the accesses on bus, updates the status counters. This status can be accessed any time during simulation.

Supported Simulators

- VCS
- NC-SIM
- ModelSim
- Questasim

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