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eMMC Verification IP

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Overview

The process of verification is getting complex with every passing year; this is due to the fact that complexities of chips are increasing. With such an increasing design complexity, verification tends to consume up to 60-80% project resources and often represents a bottleneck. Having all this in mind, SmartDV has developed number of Verification IP's, which have been created by verification engineers with decades of experience in verifying complex chips.

eMMC JESD84-A441 VIP is an advanced solution in the market for the verification of eMMC JESD84-A441 implementations. It is adherent with eMMC JESD84-A441 standard and supports 1-bit, 4-bit and 8-bit data bus width modes. It can generate all command types. The eMMC VIP monitor acts as powerful protocol-checker, fully compliant with eMMC JESD84-A441 specifications.

The SmartDV Verification IP (VIP) for eMMC provides an efficient and simple way to verify the eMMC protocol bus. It includes an extensive test suite covering all the possible scenarios and eMMC conformance norms. It can perform all protocol tests as test bench and moreover it allows an easy generation of a very high number of patterns and a set of specified patterns to stress the DUT.

- Operates as eMMC Host, eMMC Slave and eMMC Monitor.

Features

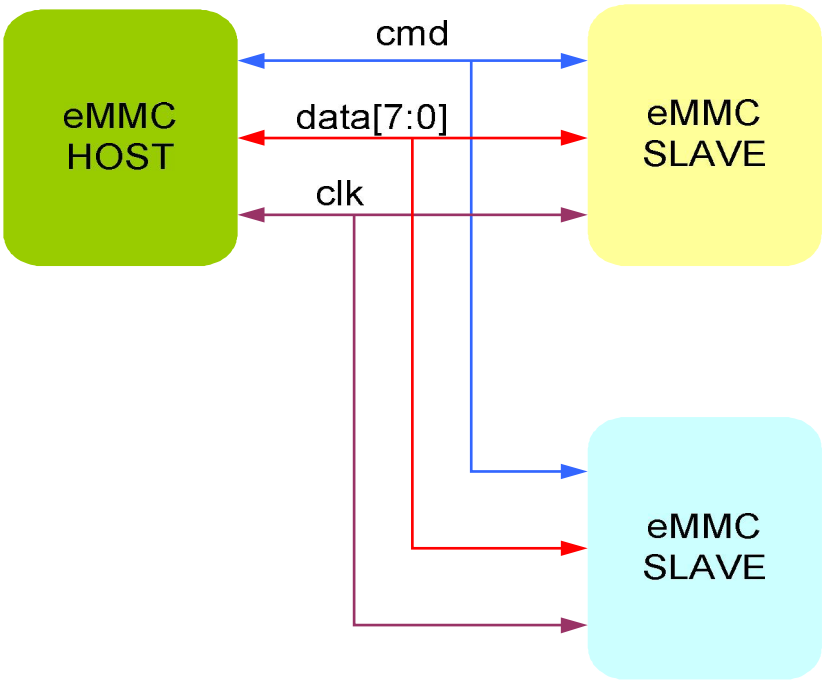
- Implemented in **Unencrypted OpenVera, SystemVerilog, Verilog, SystemC and Specman E.**
- Supported RVM, AVM, VMM, OVM, UVM and non-standard verify env.
- Supports e-MMC standard, high capacity standards JESD840A42, JESD84-A441 and MMC standard JESD840B42.
- Single byte, single block, multiple block (finite and infinite) transfers
- Supports stream transfer operations
- Supports three different data width bus modes
  - 1-bit(default)
  - 4-bit
  - 8-bit
- Supports password protection of data
- Supports simple erase mechanism
- Supports higher than 2GB of density of memories.

- Supports boot operation mode with simple boot sequence method
- Supports alternative boot operation mode
- Supports dual data rate transfer
- Supports high speed boot.
- Supports hardware reset signal
- Supports write protection features for the boot and user areas, which may be permanent, power-on or temporary
- Bus-accurate timing
- Detects and reports the following errors.
  - Out of range error
  - Address misalign error
  - CRC error
  - Switch error
  - Illegal command error
  - Block length error
  - Lock-unlock failed error
  - Erase sequence error
  - Direction bit error
  - Stuff bit error
  - Erase param error
- Protocol Checker fully compliant with JESD840A42 and JESD84-A441.
- eMMC Verification IP comes with **complete testsuite** to test every feature of eMMC specification.
- Monitors, detects and notifies the test bench of significant events such as transactions, warnings, timing and protocol violations
- Status counters for various events on bus.
- Functional coverage for complete eMMC features

Benefits

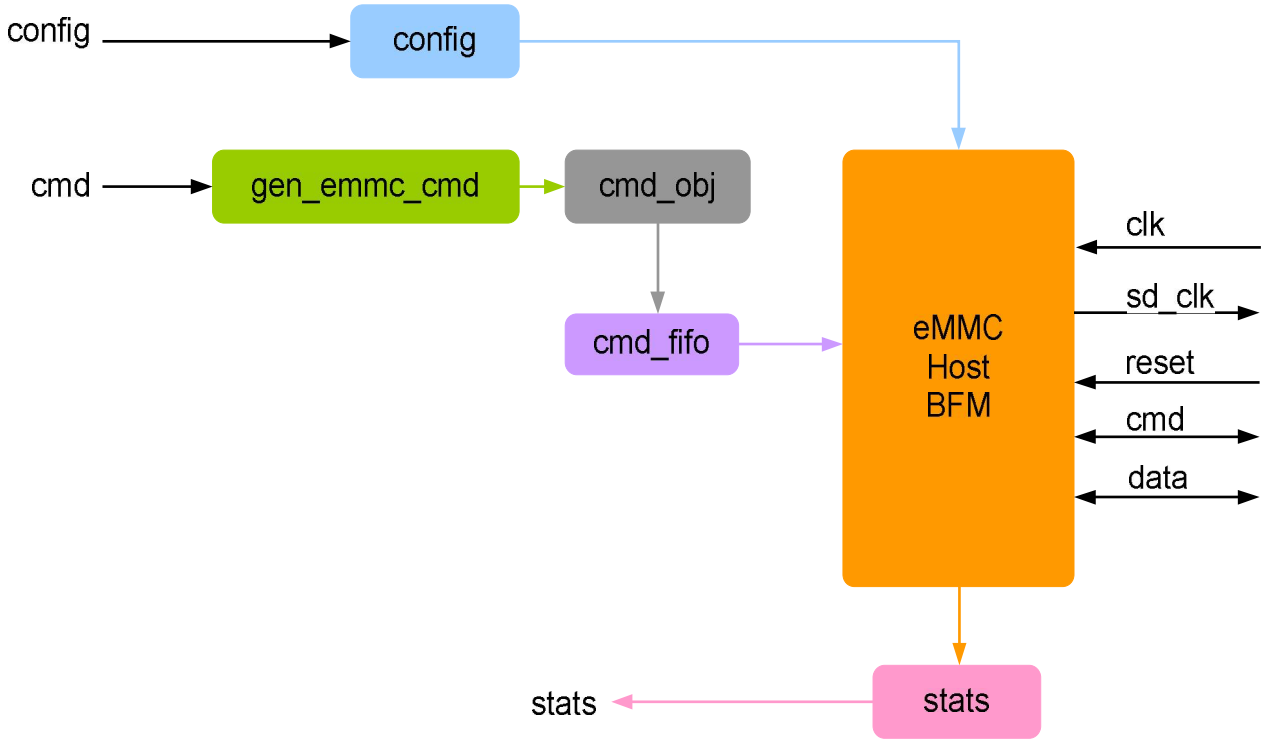
- Faster testbench development and more complete verification of eMMC designs.
- Simplifies results analysis.
- Easy to use command interface simplifies testbench control and configuration of Host and slave.
- Runs in every major simulation environment.

eMMC Verification IP Topology



Host Behavior

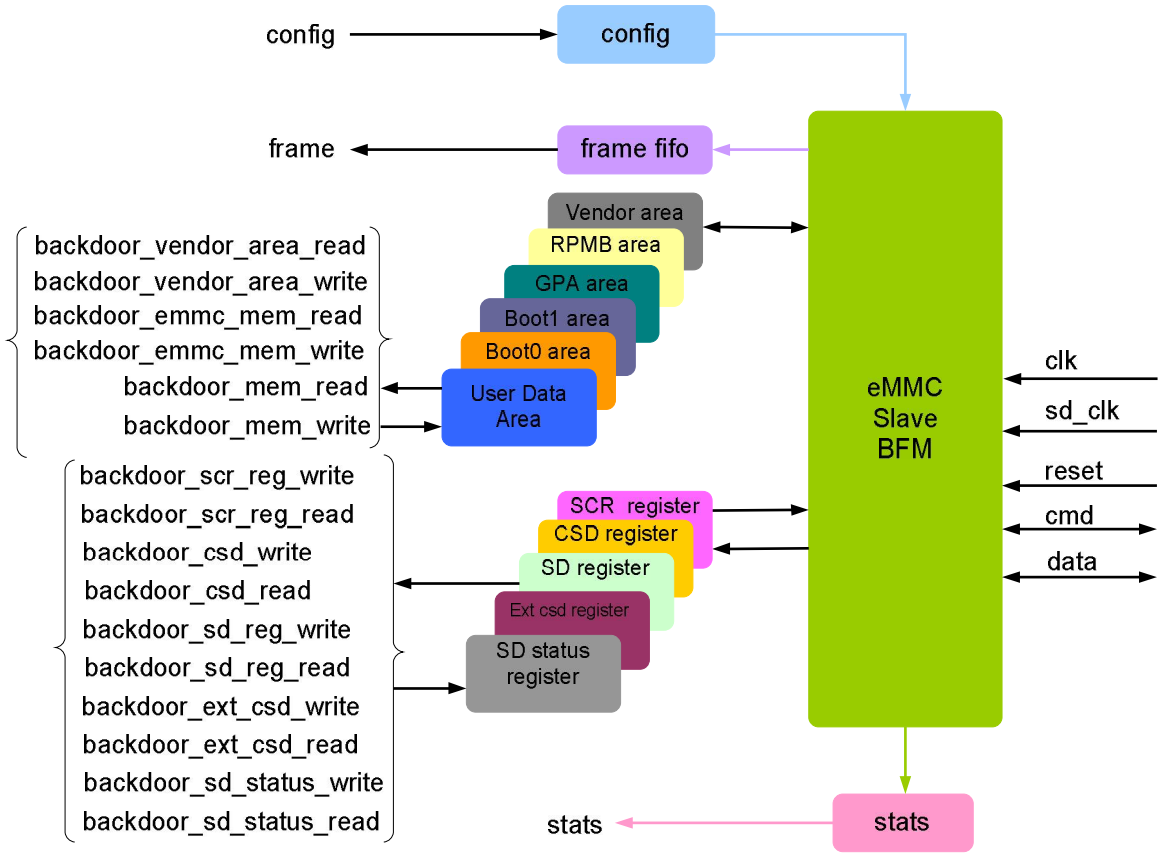
eMMC Host BFM is first configured with various configuration parameters like write data delay, command to command delay, and FIFO depth.



User has access to rich set of eMMC commands to generate various types of accesses on the eMMC bus; these commands are flexible to allow full randomization of various fields of the command. For commands that get response from the slave, they are placed in HOST frame FIFO. Status counters are updated at the end of transmission of command. Error injection is supported by forcing the host to abort the transfer at the specified position

Slave Behavior

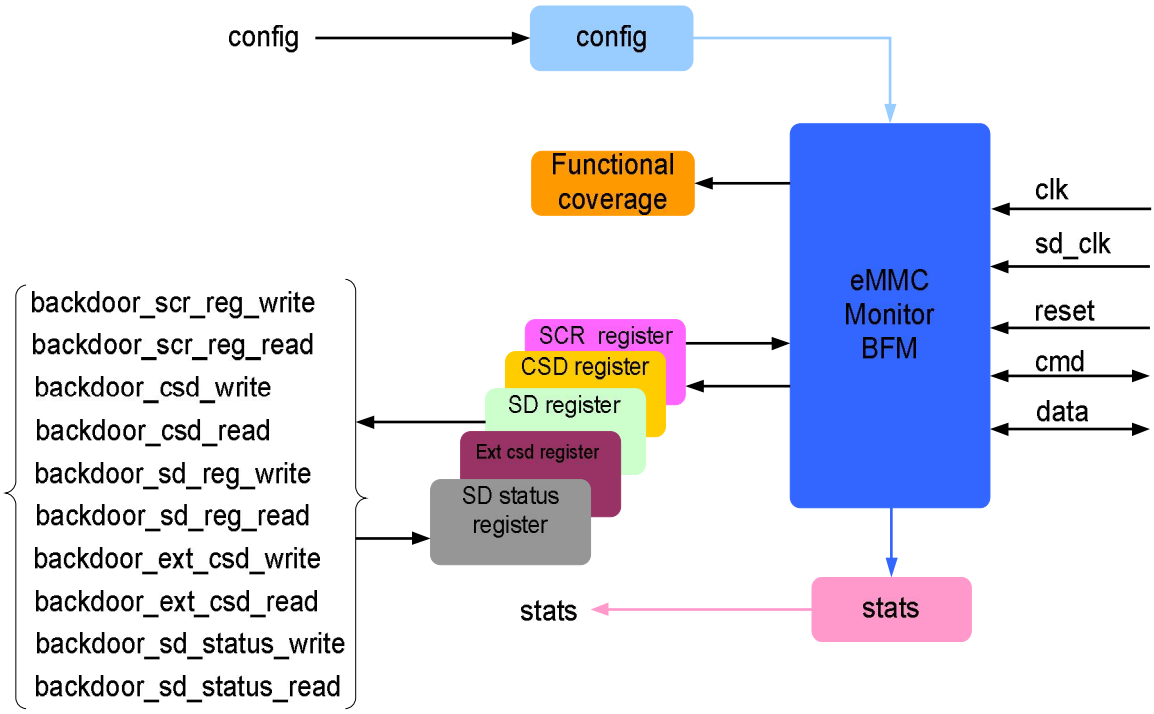
eMMC Slave is first configured with different configuration parameters. The slave keeps monitoring the bus for a valid command from the host. Depending on command type slave responds to the HOST. For a write command, slave receives data from host and writes to internal memory model. For the read command, slave sends the data to host from the memory model. Slave BFM behaves as per the device configured. At the end of command reception, status counters are updated.



Monitor Behavior

Monitor is first configured with different configuration parameters. Monitor monitors the eMMC bus for protocol errors and timing errors. Monitor also keeps track of all the accesses on the bus and updates the status counters. These status counters can be accessed any time during simulation. The monitor also implements functional coverage points which user can use to

measure the quality of verification.



Supported Simulators

- VCS
- NC-Sim
- Modelsim

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