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Ethernet Verification IP

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Overview

The process of verification is getting complex with every passing year; this is due to the fact that complexity of chips are increasing. With such an increasing design complexity, verification tends to consume up to 60-80% project resources and often represents a bottleneck. Having all this in mind, SmartDV has developed number of Verification IP's, which has been created by verification engineers with decades of experience in verifying complex chips.

The SmartDV Verification IP (VIP) for Ethernet provides an efficient and simple way to verify the 10M/100M/1G/10G/40G/100G Ethernet protocol bus. The SmartDV VIP for 10M/100M/1G/10G/40G/100G is fully compliant with IEEE 802.3 Specification and provides the following features:

- Supports full 802.3 10M/100M/1G/10G/40G/100G Ethernet specification.
- Support RGMII V2.0, SGMII V1.8, QSGMII V 1.2, RMII Rev1.2, SMII 2.1 Specification.
- Operates as 10M/100M/1G/10G/40G/100G RX/TX, and also 10M/100M/1G/10G/40G/100G monitor.

Features

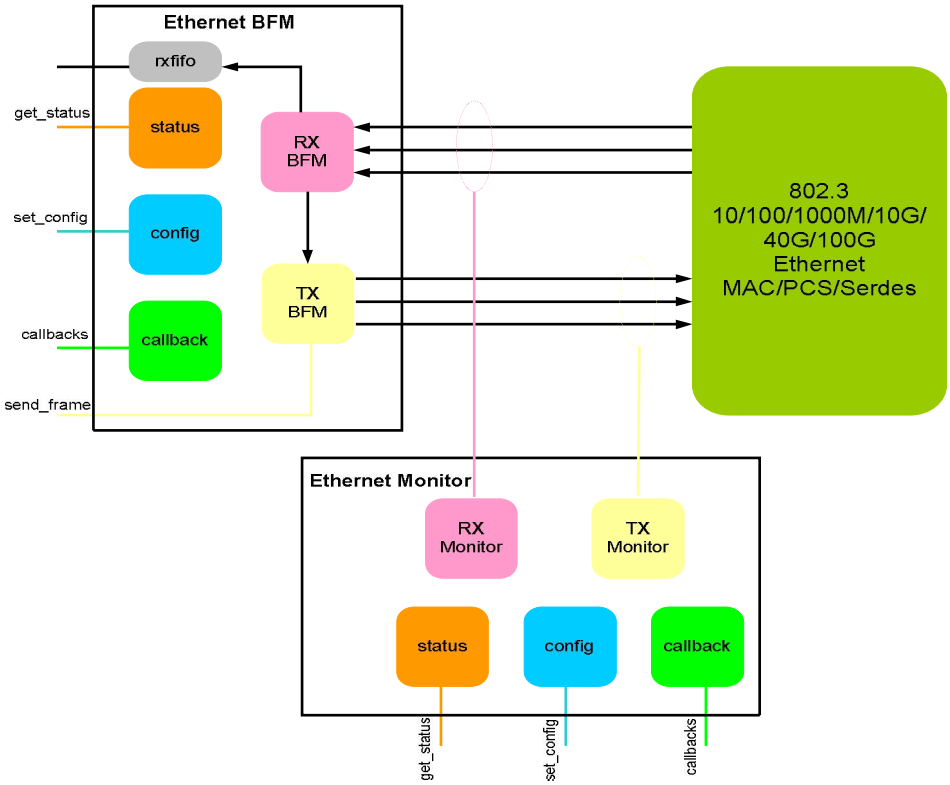
- Implemented in **Unencrypted OpenVera, Verilog, SystemC and SystemVerilog**.
- Supported RVM, AVM, **VMM**, OVM, UVM and non-standard verify env.
- Full **CGMII/00GBase-KR10/100GBase-CR10/100GBase-ER4/100GBase-LR4** TX/RX functionality as per Clause 80, Clause 81, Clause 82, Clause 83, Clause 84, Clause 85, Clause 86, Clause 88
- Full **XLGMII/40GBase-KR4/40GBase-CR4** TX/RX functionality as per Clause 80, Clause 81, Clause 82, Clause 83, Clause 84, Clause 85, Clause 86, Clause 87.
- Full **XGMII/XTBI/10GBase-KX4/XAUI/XTBI/10GBase-KR** TX/RX functionality as per Clause 46, Clause 47, Clause 48, Clause 49, Clause 54, Clause 55,
- Full **GMII/SGMII/QSGMII/RGMII/RTBI/TBI** TX/RX Functionality as per Clause 35, Clause 36.
- Full **MII/RMII/SMII** TX/RX functionality as per 802.3 specifications.
- Full support for IEEE 1588-2002 and IEEE 1588-2008
- Full support for IEEE 802.1Qat
- Full support for IEEE 802.1QAV
- Full support for IEEE 802.1Q

- Full support for IEEE 802.1AS
- Full support for IEEE 802.3BG
- Full support for IEEE 802.1AZ (Energy Efficient Ethernet)
- Supports **WAN Interface Sublayer (WIS),** type 10GBASE-W
- Supports MDIO slave and master model as per Clause 22 and Clause 45
- Support Full Duplex and Half Duplex for 10/100/1G
- Supports auto-negotiation for SGMII.
- Supports auto-negotiation as per Clause37, Clause 28 and Clause 73 for BP and 1000Base.
- Supports CDR for serial protocols.
- Mac control and data frames support
- Ability to generate VLAN tagged, Priority tagged frames.
- Supports Pause frame detection and generation.
- Supports Jumbo frames.
- **Supports 8,10,16,20,32,40 bit serdes interface**
- Supports scrambler and FEC for 10G/40G/100G Protocols as per Clause 74.
- Supports all types of error insertion and detection.
    - Under and oversize frame.
    - CRC errors
    - Framing errors
    - Pause frame errors
    - Disparity and Auto-negotiation errors
    - Invalid code group insertion
    - Invalid /K/ characters insertion
    - Lane Skew insertion
    - Invalid AN sequence error insertion
    - Missing /K/ characters for packet boundries.
- Callbacks in TX, RX and monitor for user processing of data
- Notifies the testbench of significant events such as transactions, warnings, timing and protocol violations.
- Ethernet Verification IP comes with **complete testsuite** to test every feature of Ethernet specification and also as per **UNH testsuite.**
- Functional coverage for complete 802.3 Ethernet features.

Benefits

- Faster testbench development and more complete verification of Ethernet designs.
- Simplifies results analysis.
- Integrates easily into **OpenVera, SytemVerilog,SystemC,Verilog**
- Runs in every major simulation environment
- Written in 100% systemverilog and VMM. So runs faster and easy to use with VMM testbenches.

Ethernet Verification IP Topology



Ethernet BFM Behavior

Ethernet BFM is first configured with different configuration parameters. RX BFM collects the frames in the RX path and processing them for any errors. At each stage of frame collections, callbacks are used for giving control to user to processing the frame. At the end of frame reception, status counters are updated and frame is pushed in receive FIFO for user processing.

User uses the rich set of methods for sending frames on TX path of BFM. At each stage of sending frame, callbacks are executed for giving control to user to processing the frame or error insertion, Status counter are updated at the end of transmission of frame.

When the RX BFM receives pause frame, TX BFM pauses the traffic, based on pause quanta.

Transmit BFM supports insertion of various errors, and Receive BFM supports detection of all the errors.

Monitor Behavior

Monitor is first configured with different configuration parameters. A monitor monitors the bus

for protocol errors and timing errors. Monitor also keeps track of all the access on bus, executes the callback for user to have access to data on bus, updates the status counters. these status can be accessed any time during simulation.

Monitor also implements functional coverage, which can be used for tracking quality of verification.

Supported Simulators

- VCS
- NC-SIM
- Modelsim
- Questasim

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