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FlexRay Verification IP

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Overview

The process of verification is getting complex with every passing year; this is due to the fact that complexities of chips are increasing. With such an increasing design complexity, verification tends to consume up to 60-80% project resources and often represents a bottleneck. Having all this in mind, SmartDV has developed number of Verification IP's, which has been created by verification engineers with decades of experience in verifying complex chips.

The SmartDV Verification IP (VIP) for Flexray provides an efficient and simple way to verify the FLEXRAY protocol bus. The SmartDV VIP for Flexray is fully compliant with 2.1 Specification and provides the following features:

- Supports full Flexray specification.
- Operates as Flexray node, and also Flexray monitor.

Features

- Implemented in **Unencrypted OpenVera, Verilog, SystemC, SystemVerilog and Specman E.**
- Supported RVM, AVM, VMM, OVM, UVM and non-standard verify env.
- Complete FlexRay Tx/Rx functionality.
- Support Full Duplex of operations.
- Operates as a Tx or as a Rx.
- All types of frame generation.
- Various kinds of Tx and Rx errors insertion and detection.
  - Syntax errors
    - Frame ID error (Frame ID = 0)
    - Header CRC error
    - CRC error
  - Content errors
    - Cycle Count error
    - Frame ID error
    - Startup, Sync & Null frame errors w.r.t Dynamic segment
    - Startup & Sync frame errors w.r.t Static segment
- Callbacks in TX, RX and monitor for user processing of data.
- Status counters for various events on bus.
- Monitors, detects and notifies the testbench of significant events such as transactions,

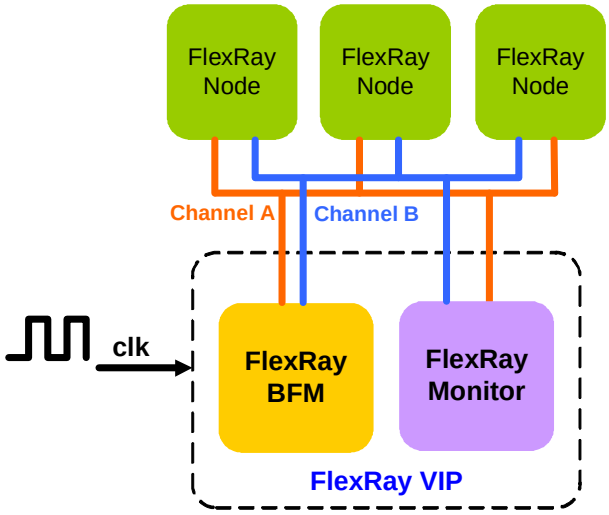
warnings, timing and protocol violations.

- FlexRay Verification IP comes with **complete testsuite** to test every feature of FlexRay specification.
- Functional coverage for complete FlexRay features.

Benefits

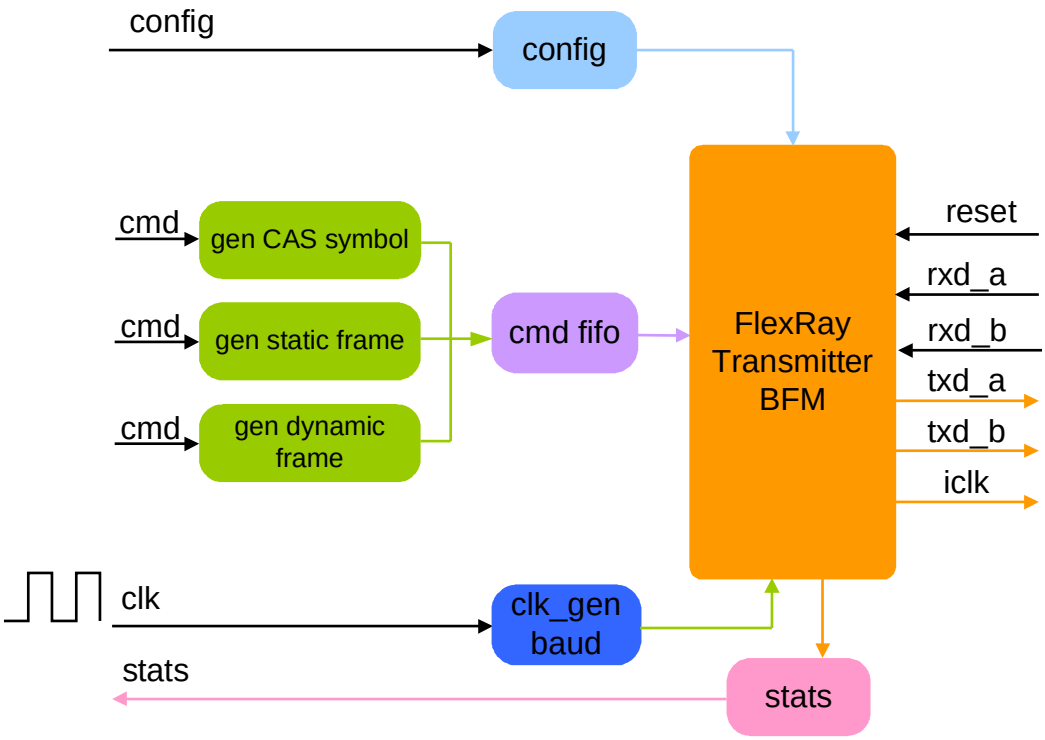
- Faster testbench development and more complete verification of Flexray designs.
- Simplifies results analysis.
- Easy to use command interface simplifies testbench control and configuration of slave and master**.**
- Runs in every major simulation environment.

Flexray Verification IP Topology



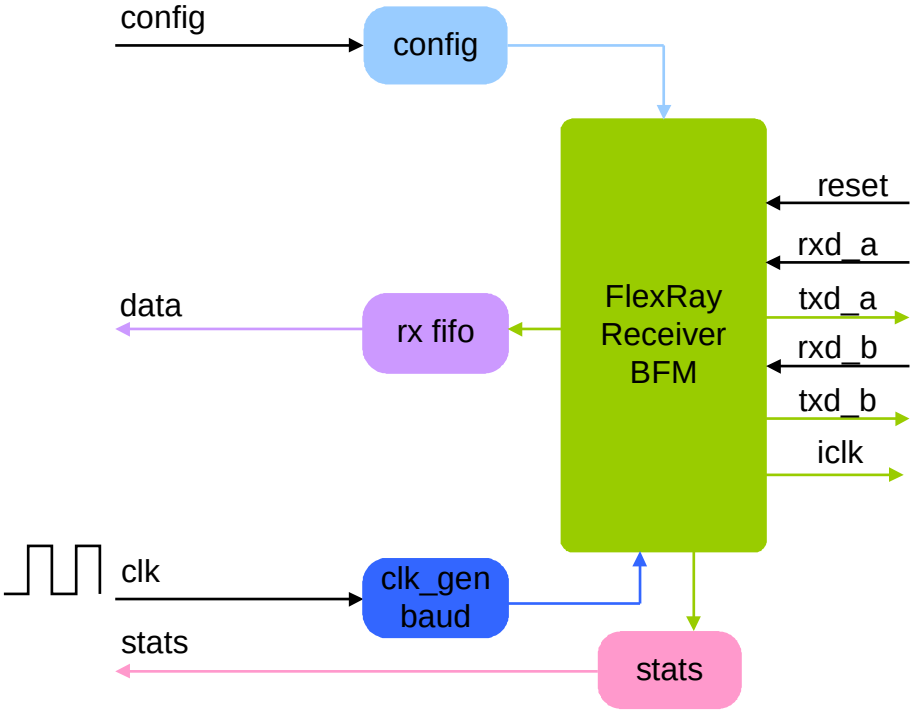
Master Behavior

Flexray Master is first configured with different configuration parameters. Flexray BFM initiates the possible requests based on the various Flexray commands from the testbench. User uses the rich set of methods for sending frames on Tx path of BFM. At each stage of sending frame, callbacks are executed for giving control to user to processing the frame. Status counters are updated at the end of transmission of frame.



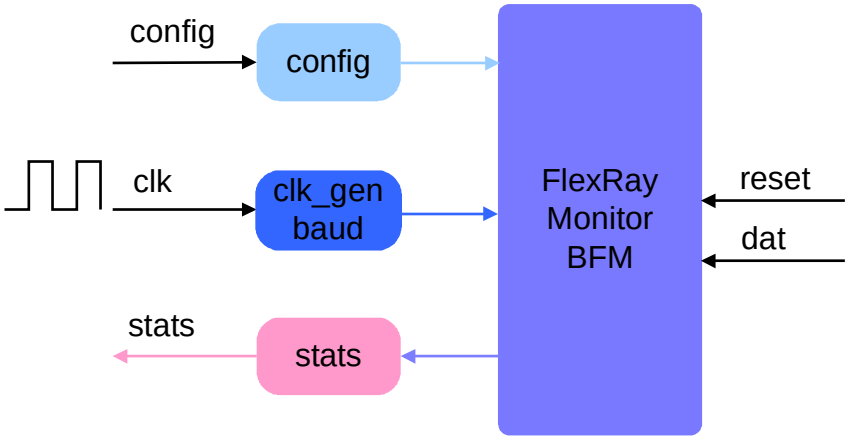
Slave Behavior

Flexray Slave is first configured with different configuration parameters. A slave device monitors the bus to determine if it has been selected for a transfer request. It will always respond to a transfer request if it has been selected. The read data on the Rx path of slave is collected in the Rx FIFO. At each stage of frame collections, callbacks are used for give control to the user to process the frame. At the end of frame reception, status counters are updated.



Monitor Behavior

Monitor is first configured with different configuration parameters. A monitor monitors the Flexray bus for protocol errors and timing errors. Monitor also keeps track of all the access on bus, executes the callback for user to have access to data on bus, updates the status counters. These status can be accessed any time during simulation.



Supported Simulators

- VCS
- NC-SIM
- ModelSim
- Questasim

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