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MIPI HSI Verification IP

Datasheet May 2011 – Version 1.02

Overview

The process of verification is getting complex with every passing year; this is due to the fact that complexities of chips are increasing. With such an increasing design complexity, verification tends to consume up to 60-80% project resources and often represents a bottleneck. Having all this in mind, SmartDV has developed number of Verification IP's, which has been created by verification engineers with decades of experience in verifying complex chips.

The SmartDV Verification IP (VIP) for MIPI HSI provides an efficient and simple way to verify the MIPI HSI protocol bus. The SmartDV VIP for MIPI HSI is fully compliant with version 1.01 of the MIPI HSI Bus Specification and provides the following features:

Features

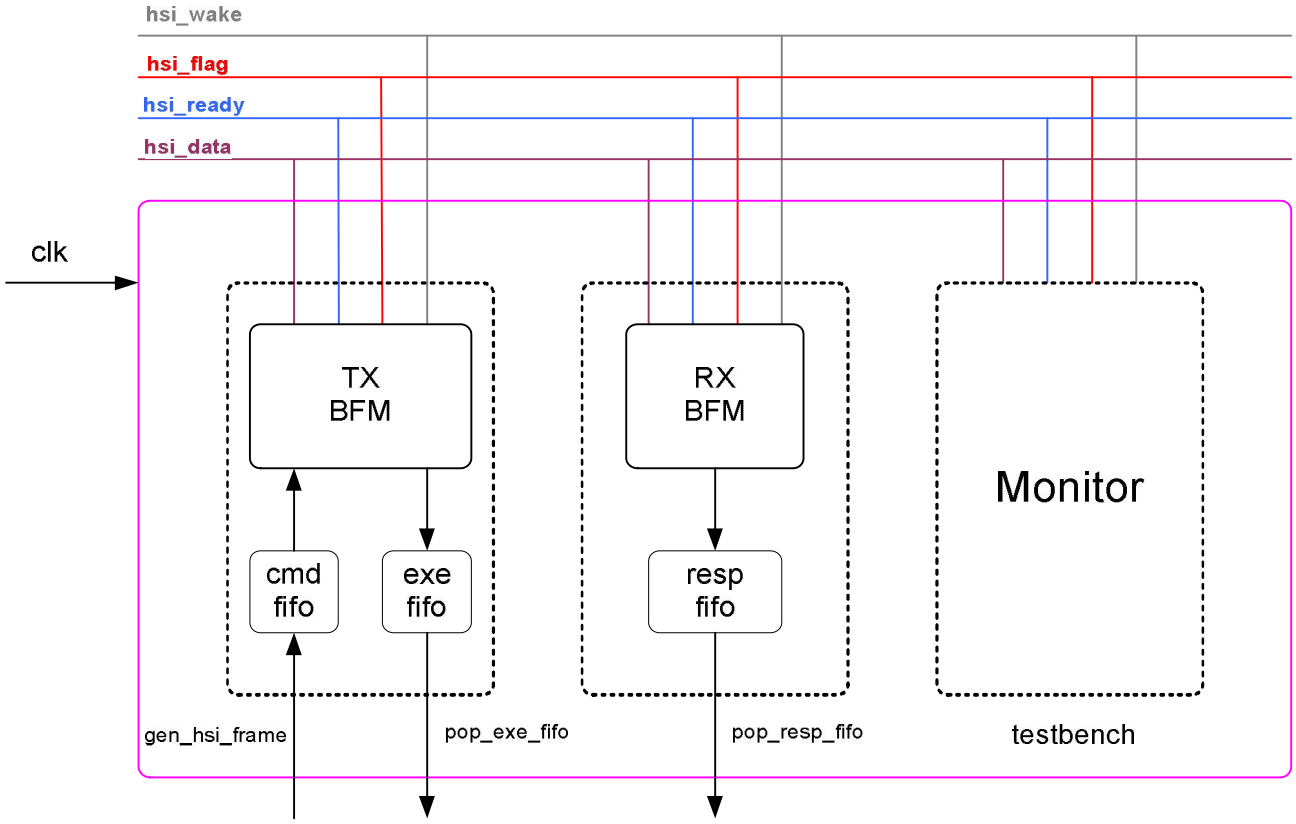
- Implemented in **Unencrypted OpenVera, SystemVerilog, Verilog, SystemC and Specman E.**
- Supported RVM, AVM, VMM, OVM, UVM and non-standard verify env.
- Supports 1.01 MIPI HSI physical layer specifications.
- Supports data flow.
  - Synchronized
  - Pipelined
  - Receiver Real Time
- Supports both type of transmission modes on transmit interface.
  - Stream transmission mode
  - Frame transmission mode
- Supports wake signal functionality.
- Error Injection Capability on Transmitter Interface.
  - Missed clock cycles
  - Additional clock cycles
  - Signal error
  - Invalid command frame error
  - Invalid message sequence error
  - Invalid channel error
  - Reserved bit error
  - Invalid response frame error
- Run-Time Configurability for transmitters.
  - Data Rate Change

- Run-Time Configurability for receivers.
  - Data rate range
  - Time-out counter ON/OFF
  - Time –out counter value
  - Tailing bit counter ON/OFF
  - Tailing bit counter value
  - Frame burst counter ON/OFF
  - Frame burst counter value
- Supports protocol.
  - Data link protocol
  - Audio protocol
- Programmable number of channels for data transfer.
- Programmable PDU length from 0 to 256 kb.
- Supports speech data frame and audio data frame.
- Resynchronization supported for data link protocol.
- Monitor detects and notifies the test bench of all protocol and timing errors.
- Supports constraints Randomization.
- Status counters for various events on bus.
- Callbacks in transmitter, receiver and monitor for user processing of data.
- MIPI HSI Verification IP comes with complete test suite to test every feature of MIPI HSI specification.
- Functional coverage for complete MIPI HSI features.

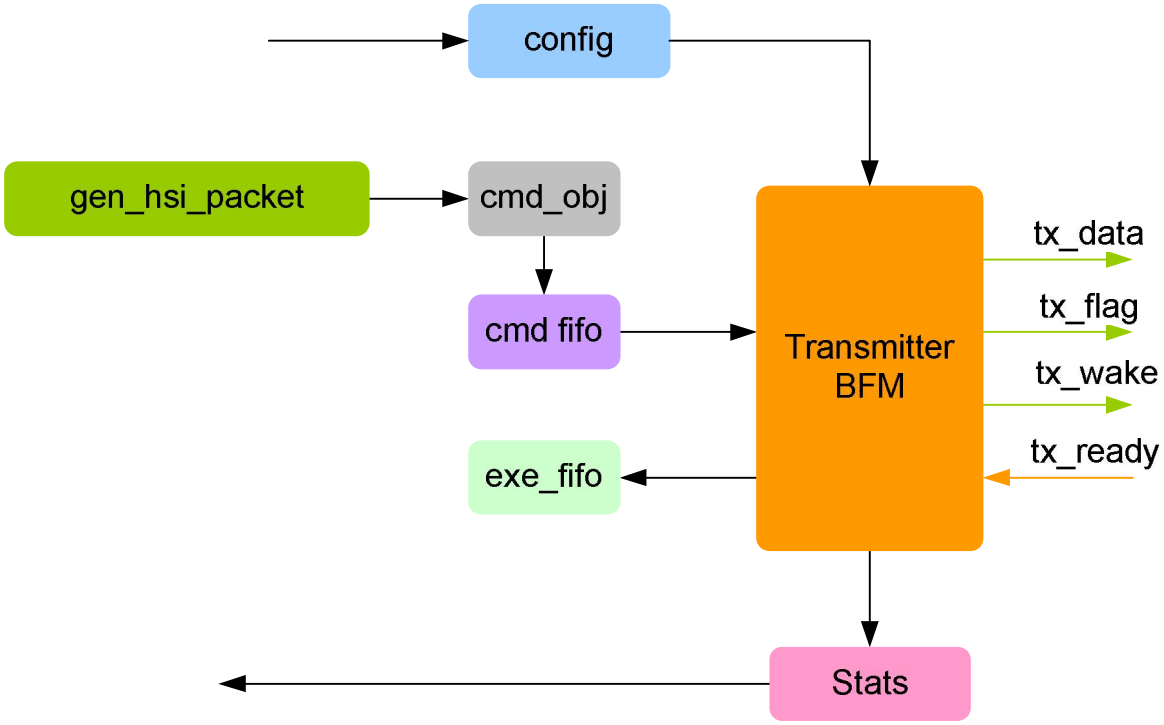
Benefits

- Faster test bench development and more complete verification of MIPI HSI designs.
- Simplifies results analysis.
- Integrates easily into **OpenVera, SytemVerilog, Verilog, Specman E, and SystemC**
- Runs in every major simulation environment

MIPI HSI Verification IP Topology



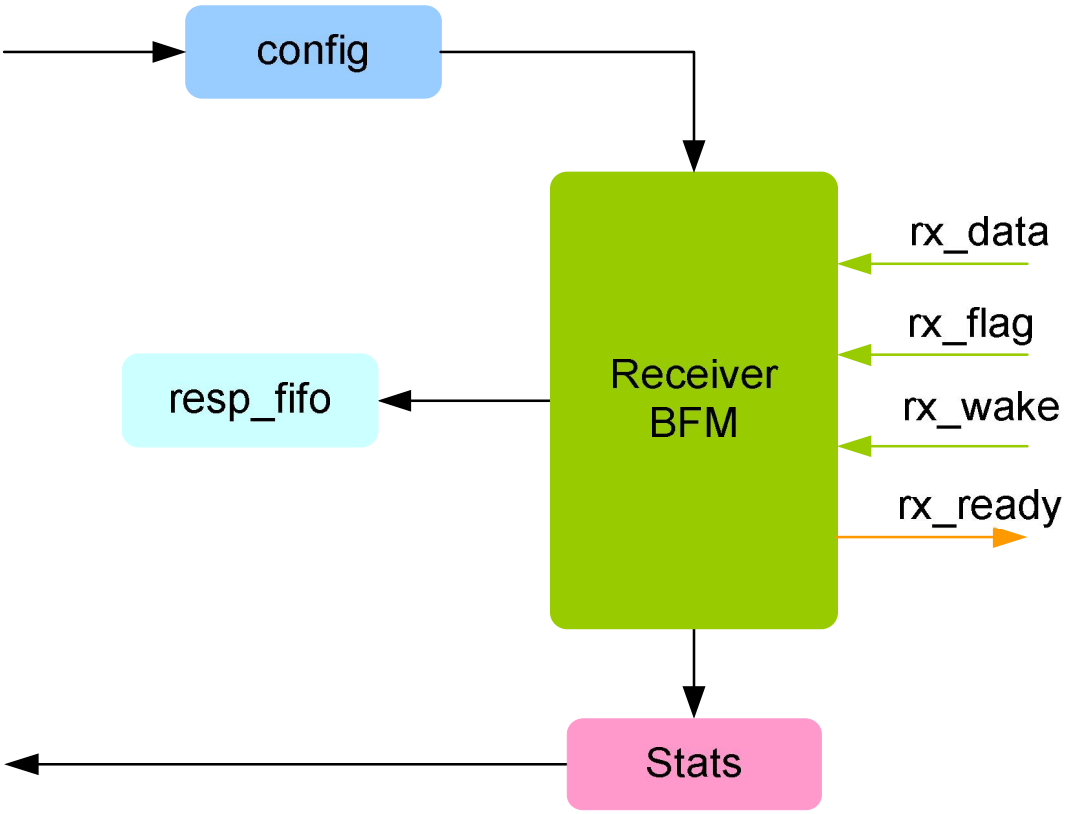
Transmitter Behavior



MIPI HSI Tx is first configured with different configuration parameters like mode, fifo depth etc. MIPI HSI BFM initiates the data flow based on MIPI HSI command from the testbench. User can use rich set of methods for sending frames on Tx path of BFM. At each stage of sending frame, callbacks are executed for giving control to user to processing the frame. Status counters are updated at the end of transmission of frame.

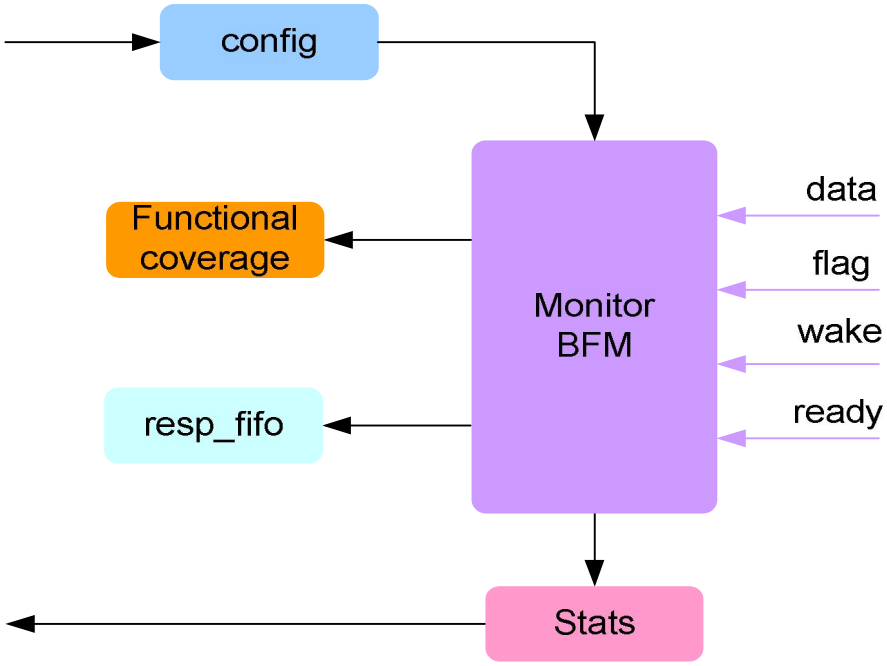
Receiver Behavior

MIPI HSI Receiver is first configured with different configuration parameters like mode, fifo depth, etc. Receiver device monitors the bus for the start of frame. After receiving the start of frame, the receiver starts receiving the frames. At each stage of frame collection, callbacks are used for to give control to the user to process the frame. At the end of frame reception, status counters are updated.



Monitor Behavior

Monitor is first configured with different configuration parameters like mode, fifo depth, etc. A monitor monitors the MIPI HSI bus for protocol errors and timing errors. Monitor also keeps track of all the accesses on bus, updates the status counters. These statuses can be accessed any time during simulation. Monitor also implemented the functional coverage points which user can extend to add or remove new functional coverage points.



Supported Simulators

- VCS
- NC-SIM
- Modelsim
- Questasim

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