Smart DV Technologies India Private Limited
14/B, 2nd Cross, SR Layout,
Bangalore, India : 560017
E-Mail : info@smart-dv.com
http://www.smart-dv.com

I2C Verification IP

Datasheet July 2011 – Version 2.0

Overview

The process of verification is getting complex with every passing year; this is due to the fact that complexity of chips are increasing. With such an increasing design complexity, verification tends to consume up to 60-80% project resources and often represents a bottleneck. Having all this in mind, SmartDV has developed number of Verification IP's, which has been created by verification engineers with decades of experience in verifying complex chips.

The SmartDV Verification IP (VIP) for I2C provides an efficient and simple way to verify the I2C bidirectional two-wire bus. The SmartDV VIP for I2C is fully compliant with version 3.0 of the Philip's I2C Bus Specification and provides the following features:

- Supports standard, fast, and high speed operations. The model has a rich set of configuration parameters to set clock synchronization and generation of the Serial Clock Line (SCL) to meet all clocking requirements.
- Operates as a Master, Slave. As a Master, the model can Start/Stop all possible transfers. In addition, as a Slave device it can detect Start/Stop conditions and perform data transfers according to the initiator request.

Features

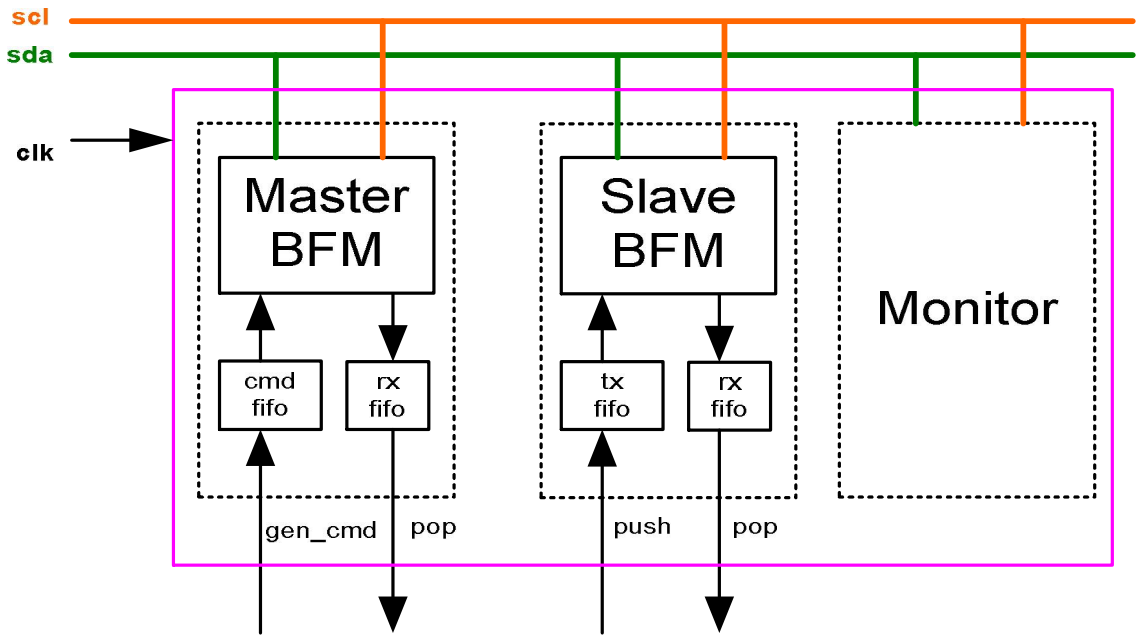
- Implemented in **Unencrypted OpenVera, Verilog, SystemC and SystemVerilog**.
- Supported RVM, AVM, **VMM**, OVM, UVM and non-standard verify env.
- Full I2C Master and Slave functionality.
- Start, repeat start and stop for all possible transfers.
- Supports all I2C clocking speeds, Including HS mode.
- 7b/10b configurable slave address.
- Allows testing of varies bus traffic for Read, Write, General Call and CBUS.
- Supports complex sequence of 7/10 bit with repeated start command sequences.
- Bus-accurate timing.
- Supports START byte generation and handling.
- Supports master/slave arbitration and clock synchronization.
- Glitch insertion and detection.
- Callbacks in master, slave and monitor for user processing of data
- Supports insertion of errors
    - Master abort in middle of transaction.
    - ACK on last read phase.

    - Master continue on NACK after write NACK from slave.
    - Random and Periodic clock period stretching by slave.
    - Random Write NACK insertion by slave.
- Notifies the testbench of significant events such as transactions, warnings, timing and protocol violations.
- Functional coverage of complete I2C specs.
- I2C Verification IP comes with **complete testsuite** to test every feature of I2C specification.

Benefits

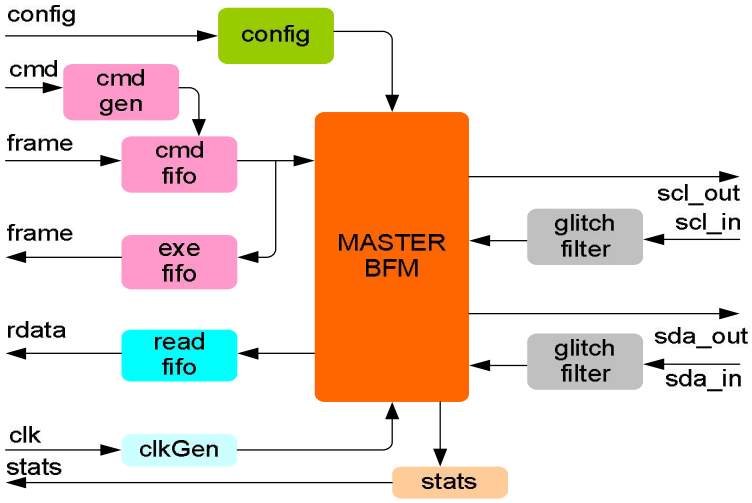
- Faster testbench development and more complete verification of I2C designs.
- Simplifies results analysis.
- Integrates easily into **OpenVera, SytemVerilog, Verilog, Specman, SystemC.**
- Runs in every major simulation environment

I2C Verification IP Topology



Master Behavior

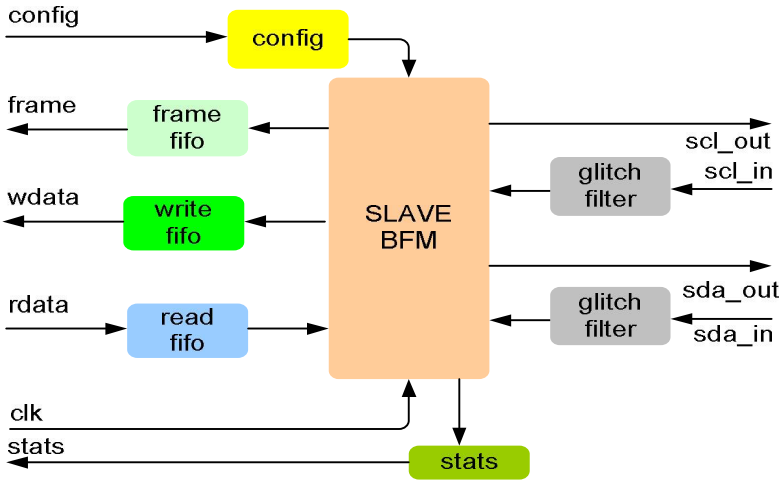
Each master is first configured with different configuration parameters. The master then initiates requests based on read,write and general call transfers from the testbench. Read data from slave is placed in RX Fifo.



The master also arbitrates the bus using the serial data (SDA) and SCL lines and can be configured to react in different ways if the bus is not free. Arbitration follows the rules set by the I2C protocol. Error injection is supported by forcing the Master to abort the transfer at the specified bit position or sending ACK on last byte of write.

Slave Behavior

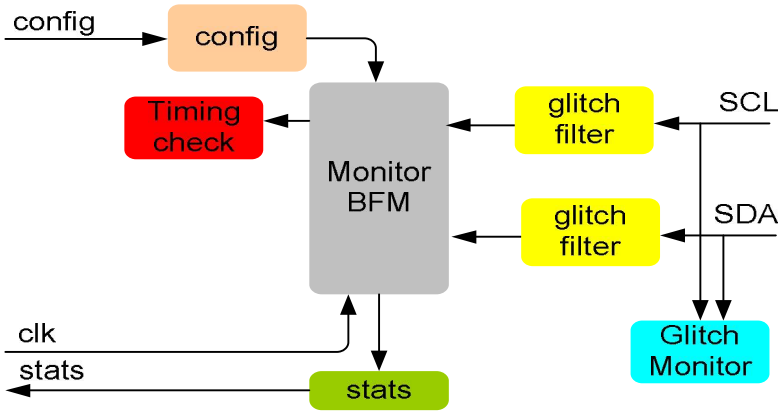
Each slave is first configured with different configuration parameters. A slave device monitors the bus to determine if it has been selected for a transfer request. It will always respond to a transfer request if it has been selected. The slave responds to read requests by sending data which can be fed through its TX Fifo. For write requests, the slave receives data transmitted by the master and passes it to the RX fifo.



The slave can be made to act erroneously by forcing it to respond with an acknowledgment (or no acknowledgment) to transfer requests. Slave BFM supports user callbacks for read and write command processing.

Monitor Behavior

Monitor is first configured with different configuration parameters. A monitor monitors the I2C bus for protocol errors and timing errors.



Monitor also keeps track of all the access on bus, and this stats can be accessed any time during simulation.

Supported Simulators

- VCS
- NC-Sim
- Modelsim
- Questasim

Smart DV Technologies India Private Limited
14/B, 2nd Cross, SR Layout,
Bangalore, India : 560017
E-Mail : info@smart-dv.com
http://www.smart-dv.com