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I2S Verification IP

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Overview

The process of verification is getting complex with every passing year; this is due to the fact that complexity of chips are increasing. With such an increasing design complexity, verification tends to consume up to 60-80% project resources and often represents a bottleneck. Having all this in mind, SmartDV has developed number of Verification IP's, which has been created by verification engineers with decades of experience in verifying complex chips.

The SmartDV Verification IP (VIP) for I2S provides an efficient and simple way to verify the I2S protocol bus. The SmartDV VIP for I2S is fully compliant with version 1.1 of the Philip's I2S Bus Specification and provides the following features:

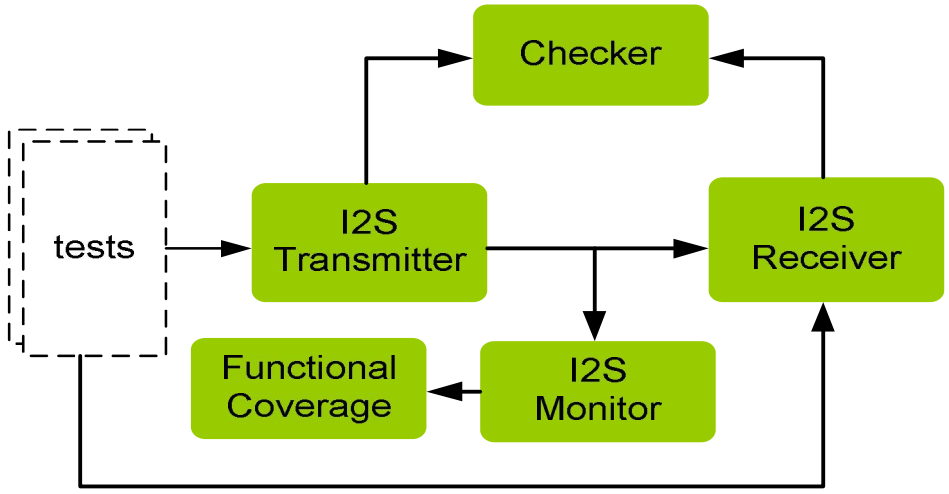
Features

- Implemented in **Unencrypted OpenVera, SystemVerilog, Verilog, SystemC and Specman E.**
- Supported RVM, AVM, VMM, OVM, UVM and non-standard verify env.
- Full I2S Transmitter and Receiver functionality.
- Complies with Philips Inter-IC Sound Bus Specification.
- Data word-lengths of 8, 10, 12, 14, 16, 18, 20, 24 and 32 bits.
- Supports configurable clock rate.
- Can operate as master or slave in several configurations
  - Master or slave mode as transmitter
  - Master or slave mode as receiver
  - Master mode as controller (does not transmit or receive data)
- Monitors, detects and notifies the testbench of significant events such as transactions, warnings, timing and protocol violations.
- Status counters for various events on bus.
- I2S Verification IP comes with complete test suite to test every feature of I2S specification.
- Callbacks in transmitter, receiver and monitor for user processing of data.
- Supports constraints Randomization.
- Functional coverage for complete I2S features.

Benefits

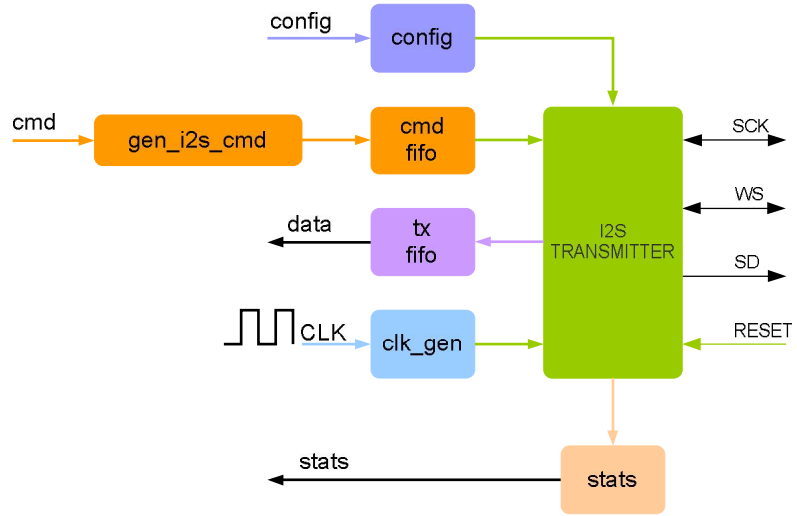
- Faster testbench development and more complete verification of I2S designs.
- Simplifies results analysis.
- Integrates easily into **OpenVera, SytemVerilog, Verilog, Specman E, and SystemC**.
- Runs in every major simulation environment.

I2S Verification IP Topology



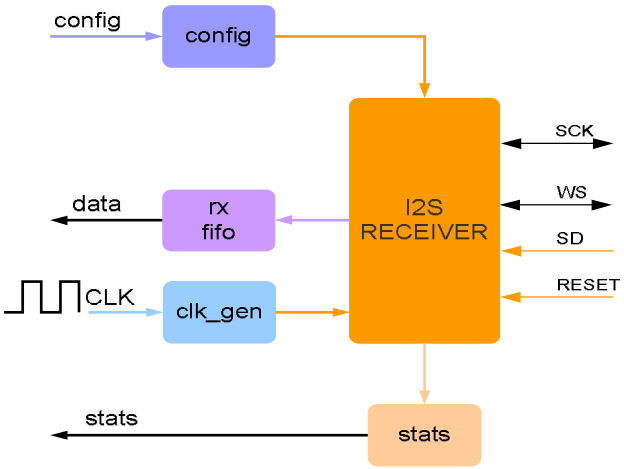
Transmitter Behavior

I2S Transmitter is first configured with different configuration parameters. I2S Transmitter initiates the possible frames based on the various I2S commands from the testbench. User uses the rich set of methods for sending frames. At each stage of sending frame, callbacks are executed for giving control to user to processing the frame. Status counters are updated at the end of transmission of frame.



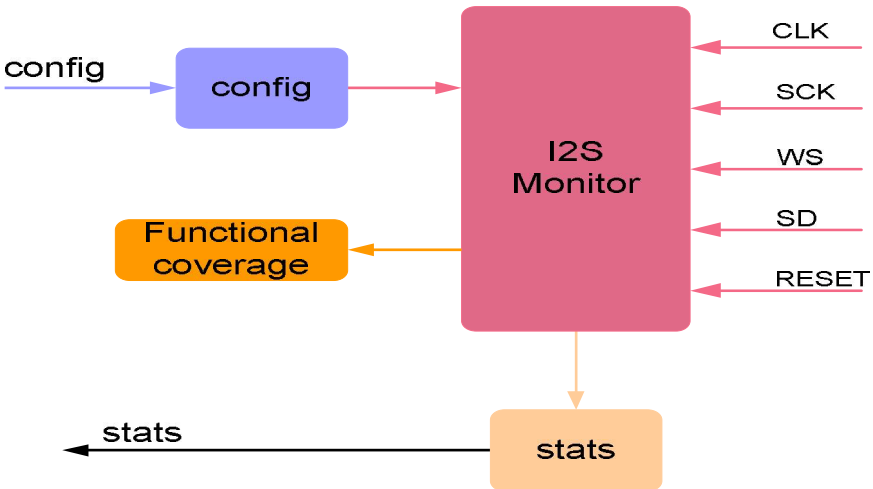
Receiver Behavior

I2S Receiver is first configured with different configuration parameters. A Receiver device monitors the bus to determine the data transaction. At each stage of frame collections, callbacks are used for give control to the user to process the frame. At the end of frame reception, status counters are updated.



Monitor Behavior

Monitor is first configured with different configuration parameters. A monitor monitors the I2S bus for protocol errors and timing errors. Monitor also keeps track of all the accesses on bus, updates the status counters. These stats can be accessed any time during simulation. The Monitor also logs all transactions into a file that can be configured through the use of log methods.



Supported Simulators

- VCS
- NC-SIM
- ModelSim
- Questasim

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