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IEC7816 Verification IP

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Overview

The process of verification is getting complex with every passing year; this is due to the fact that complexities of chips are increasing. With such an increasing design complexity, verification tends to consume up to 60-80% project resources and often represents a bottleneck. Having all this in mind, SmartDV has developed number of Verification IP's, which has been created by verification engineers with decades of experience in verifying complex chips.

The SmartDV Verification IP (VIP) for IEC7816 provides an efficient and simple way to verify the IEC7816 protocol bus. The SmartDV VIP for IEC7816 is fully compliant with the ISO/IEC7816 Bus Specification and provides the following features:

Features

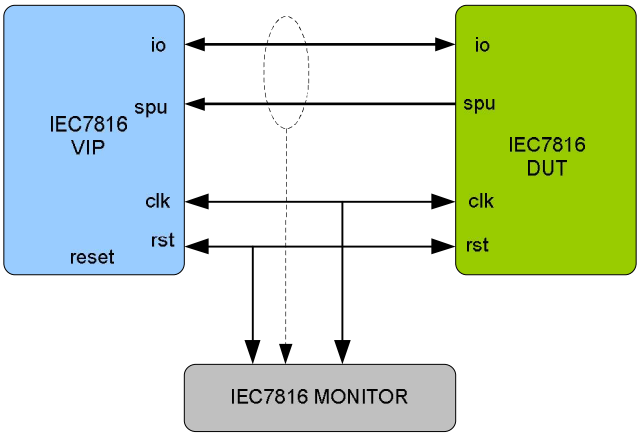
- Implemented in **Unencrypted OpenVera, Verilog, SystemC, SystemVerilog and Specman E.**
- Supported RVM, AVM, VMM, OVM, UVM and non-standard verify env.
- Adherent to ISO/IEC 7816-3 Specification.
- Complete IEC7816-3 Master/Slave functionality.
- Complete **SmartCard and SIM Card** commands supported.
- Supports all functions for complete smart card sessions, including
  - Card activation and deactivation
  - Cold/warm reset
  - Answer to Reset (ATR) response reception
  - Data transfers to and from the card
- Supports adjustable clock rate and bit (baud) rate.
- Supports configurable automatic byte repetition.
- Supports commonly used communication protocols
  - T=0 for asynchronous half-duplex character transmission, and
  - T=1 for asynchronous half-duplex block transmission
- Supports Sleep mode and Clock stop mode.
- Supports automatic convention detection.
- Supports automatic voltage class selection.
- Supports Configurable timing functions.
  - Smart card activation time
  - Guard time
  - Timeout timers

- Supports all three resynchronization levels for the Interface device of the transmission protocol.
  - Retransmission of blocks
  - Use of S(RESYNCH request)
  - Warm reset or deactivation
- Supports all three resynchronization levels for the Card of the transmission protocol.
  - Retransmission of blocks
  - Use of S(RESYNCH response)
  - Without action by the interface device, the card becomes unresponsive
- Supports all types of error insertion and detection.
  - Character parity error(s)
  - Redundancy code error
  - Invalid PCB
  - Invalid LEN
  - Loss of synchronization
  - Failure to receive the relevant S(response) after having transmitted S(request)
- Monitors, detects and notifies the testbench of significant events such as transactions, warnings, timing and protocol violations.
- Slave/Card BFM supports some standard **SmartCard and SIM Card chips.**
- Supports constraints Randomization.
- Status counters for various events on bus.
- Callbacks in transmitter, receiver and monitor for user processing of data.
- IEC7816 Verification IP comes with complete test suite to test every feature of IEC7816 specification.
- Functional coverage for complete IEC7816 features.

Benefits

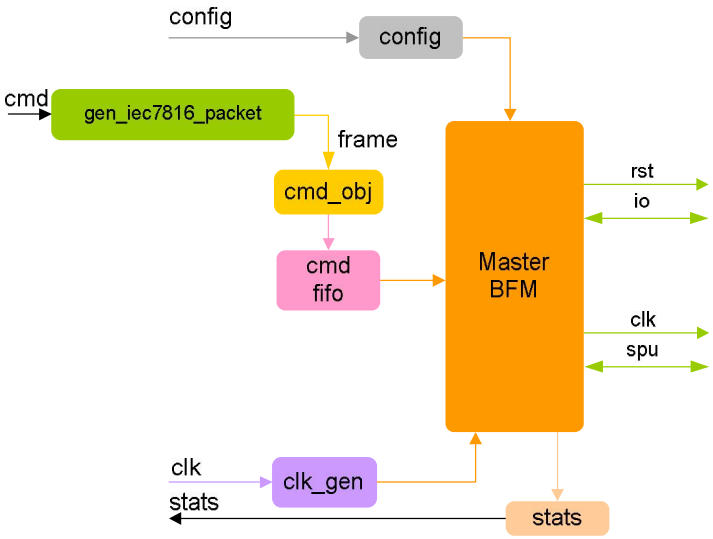
- Faster testbench development and more complete verification of IEC7816 designs.
- Simplifies results analysis.
- Integrates easily into **OpenVera, SytemVerilog, Verilog, Specman E, and SystemC.**
- Runs in every major simulation environment

IEC7816 Verification IP Topology



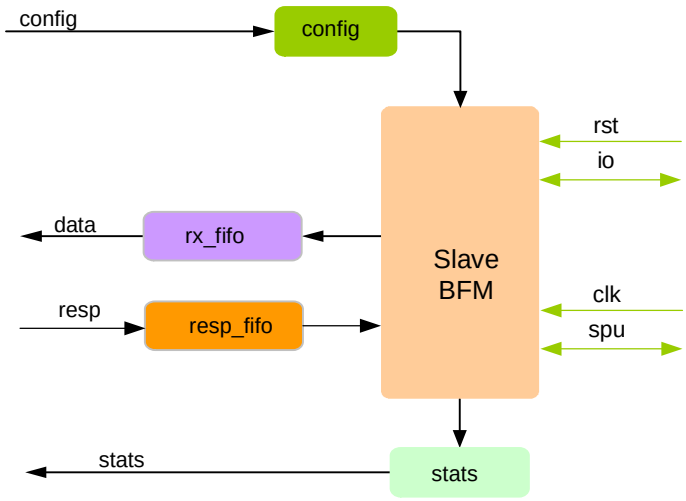
Master Behavior

IEC7816 master is first configured with different configuration parameters. IEC7816 BFM initiates the possible frames based on the various IEC7816 commands from the testbench. User uses the rich set of methods for sending frames on master transmit path of BFM. At each stage of sending frame, callbacks are executed for giving control to user to processing the frame. Status counters are updated at the end of transmission of frame.



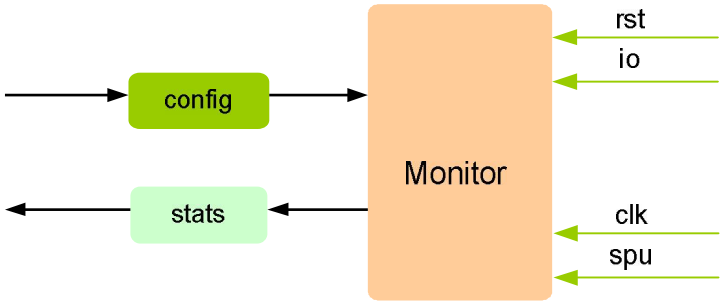
Slave Behavior

IEC7816 Receiver is first configured with different configuration parameters. A Receiver device monitors the bus to determine the data transaction. At each stage of frame collections, callbacks are used for give control to the user to process the frame. At the end of frame reception, status counters are updated.



Monitor Behavior

Monitor is first configured with different configuration parameters. A monitor monitors the IEC7816 bus for protocol errors and timing errors. Monitor also keeps track of all the accesses on bus, updates the status counters. These statuses can be accessed any time during simulation. Monitor also implemented the functional coverage points which user can extend to add or remove new functional coverage points.



Supported Simulators

- VCS
- NC-SIM
- ModelSim
- Questasim

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