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Interlaken Verification IP

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Overview

The process of verification is getting complex with every passing year; this is due to the fact that complexities of chips are increasing. With such an increasing design complexity, verification tends to consume up to 60-80% project resources and often represents a bottleneck. Having all this in mind, SmartDV has developed number of Verification IP's, which has been created by verification engineers with decades of experience in verifying complex chips.

The SmartDV Verification IP (VIP) for Interlaken provides an efficient and simple way to verify the Interlaken protocol. The SmartDV VIP for Interlaken is fully compliant with Interlaken Protocol Specification v1.2 and provides the following features:

- The model has a rich set of configuration parameters to control Interlaken functionality.
- Ability to detect and insert various types of error.

Features

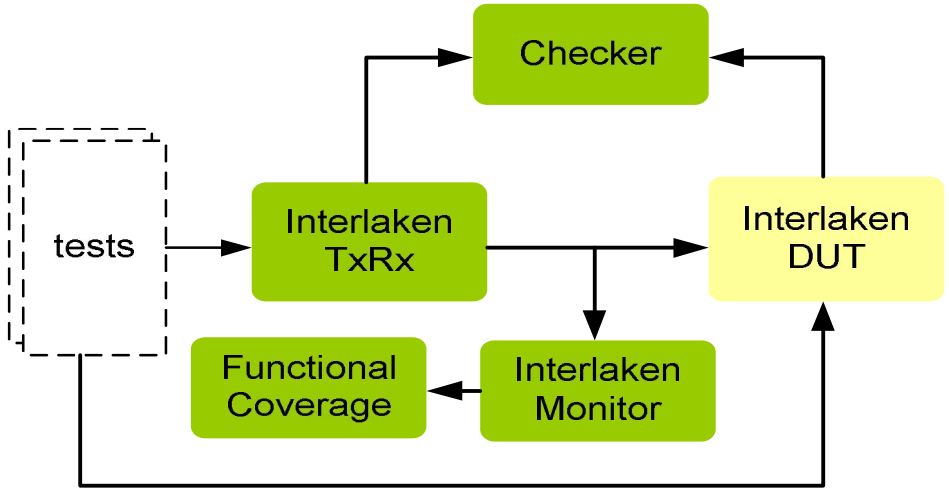
- Implemented natively in OpenVera, Verilog, SystemC, Specman E and SystemVerilog.
- Supported RVM, AVM, VMM, OVM, UVM and non-standard verify env.
- Compliant to Interlaken protocol specification v1.2.
- Compliant to Interlaken look aside protocol 1.0
- Compliant to Interlaken retransmission extension specification 1.1
- Supports multi-channel implementation as per the specification.
- Supports configurable number of serial lanes as per the specification
- Supports configurable burst max and burst short sizes.
- Supports insertion of extra idle to guarantee the avoidance of burst short.
- Supports scheduling calendar logic in the transmitter to choose the order in which the channels are serviced.
- Supports optional scheduling enhancement to avoid unused bandwidth by using decision algorithm.
- Each burst of transmitting data is encapsulated with burst control words before and after the data.
- Supports configurable metaframe length.
- Support configurable number of lanes from 1 to 64 lanes.
- Supports per channel inband and out of band flow control or both.
- Per-lane CRC-32 insertion into diagnostic words.
- Per lane skew insertion to test lane alignment.
- Configurable control to enable or disable the scrambler.

- 64B/67B encoding with inversion bits controllable.
- Variable test pattern generation as per specification.
- Supports very flexible way to test sync and alignment for state machines at startup.
- Following error injection is supported
    - Receive SerDes loses lock.
    - Receive logic loses word boundary sync.
    - Bad scrambler state.
    - Lane alignment failure.
    - Burst CRC24 Errors.
    - Flow Control Errors.
    - Unknown Control Word Types.
    - Bad 64B/67B Code words.
    - Diagnostic CRC32 Errors.
    - All types of CRC error injection.
    - Invalid coding for all control words.
    - Error injection in metaframes.
    - Short burst error injection.
    - Invalid burst boundary
- Rich set of configuration parameters to control Interlaken functionality.
- Supports 67 bit bus per lane or 1 bit serial lane to ease the debugging.
- Supports 80,64,32, 20,16,10 and 8 bit per lane serdes interface
- On-the-fly protocol and data checking.
- Notifies the testbench of significant events such as transactions, warnings, timing and protocol violations.
- Complete **functional coverage** for both normal and error cases.
- Callbacks in Transmit, receiver and monitor for various events.
- Status counters for various events on bus.
- Interlaken Verification IP comes with **complete testsuite** to test every feature of Interlaken protocol specification.

Benefits

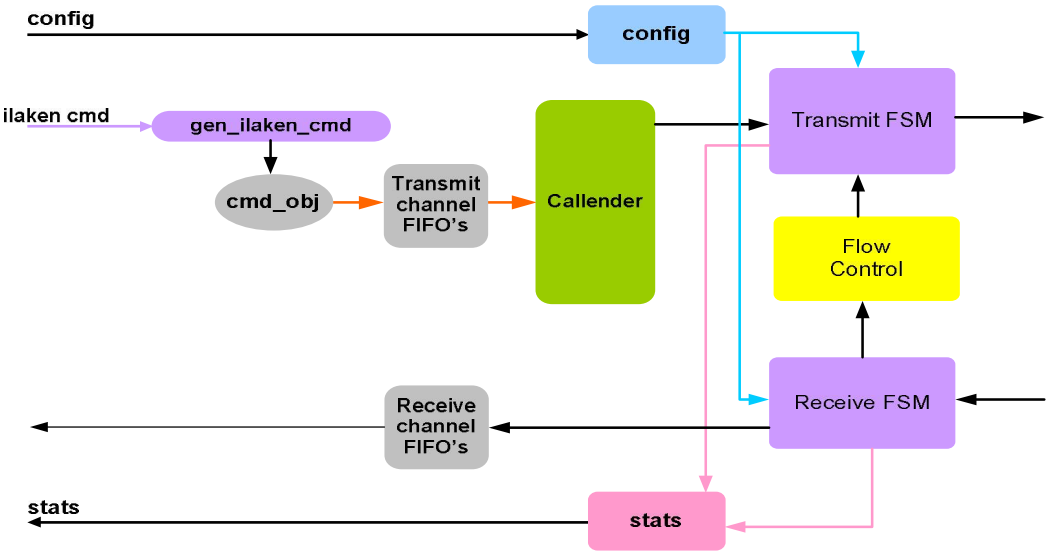
- Faster testbench development and more complete verification of Interlaken designs.
- Simplifies results analysis.
- Integrates easily into OpenVera, SystemVerilog, SystemC, Verilog
- Runs in every major simulation environment

Interlaken Verification IP Topology



BFM Behavior

Interlaken bfm is first configured with different configuration parameters. Once BFM has started, transmitter starts sending IDLE sequences to achieve synchronization. Once receiver is in sync, BFM is ready to send frames generated by the user. Whenever there is no data available to send transmitter keeps sending IDLE sequences to covey the channel availability and flow control information. Transmitter services the channel based on scheduler logic. User is provided with rich set of commands for generating data of various sizes and with various configurations.

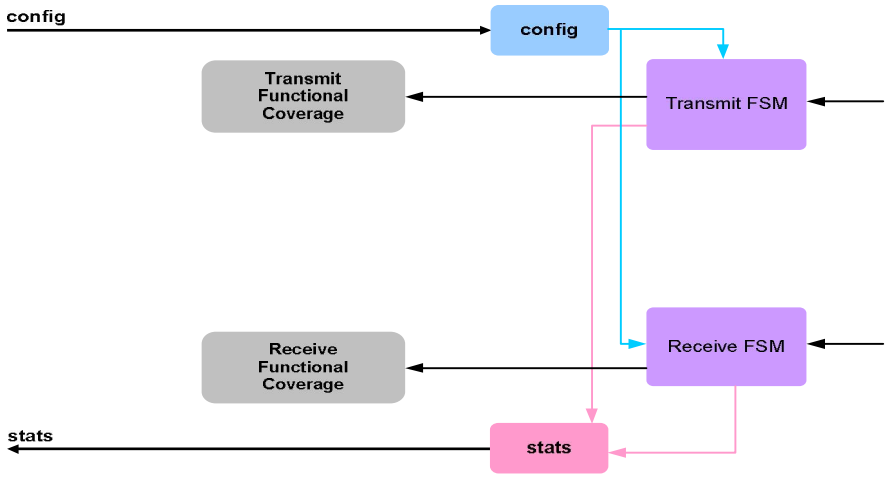


Receiver once it is in sync and deskew is done, then it collects all the frames/words and passed on to user. There are per channel fifo for user to collect the frames. There is

programmable thread running inside the receiver, which is used for generating the automatic flow control. Flow control can also be sent based on user request.

Monitor Behavior

Monitor is first configured with different configuration parameters. A monitor monitors the bus for protocol errors and timing errors. Monitor also keeps track of all the accesses on bus and these stats can be accessed any time during simulation. All transfer attributes are stored in a buffer that can be obtained using rich set of buffer commands. The Monitor also logs all transactions into a file that can be configured through the use of methods.



Monitor implements the functional coverage, which user can modify to add more coverage in object oriented way.

Supported Simulators

- VCS
- NC-SIM
- Modelsim
- Questasim

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