Smart DV Technologies India Private Limited
14/B, 2nd Cross, SR Layout,
Bangalore, India : 560017
E-Mail : info@smart-dv.com
http://www.smart-dv.com

JESD204 Verification IP

Datasheet March 2011 – Version 2.2

Overview

The process of verification is getting complex with every passing year; this is due to the fact that complexity of chips is increasing. With such an increasing design complexity, verification tends to consume up to 60-80% project resources and often represents a bottleneck. Having all this in mind, SmartDV has developed number of Verification IP's, which has been created by verification engineers with decades of experience in verifying complex chips.

The SmartDV Verification IP (VIP) for JESD204 provides an efficient and simple way to verify JESD204A protocol bus. The SmartDV VIP for JESD204 Verification IP is fully compliant with JESD204 revision A and provides following features:

- Supports JESD204 revision A/B specification.
- Operates as RAW/TBI/SERIAL RX/TX and RAW/TBI/SERIAL monitor.

Features

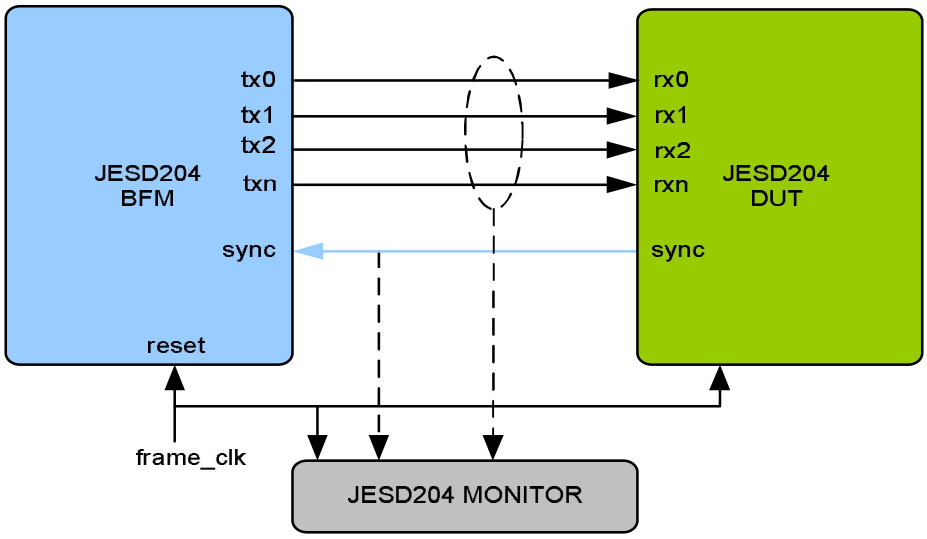
- Implemented natively in OpenVera, Specman E, SystemC, Verilog and SystemVerilog
- Natively works with VMM, RVM, OVM, UVM, RVM and AVM.
- Follows JESD204A/B specification as defined in JESD204A/B
- Supports Transmitter and Receiver Mode
- Supports up to 32 lanes
- Supports 32bit data width per converter
- Supports up to 32 converters per transmitter & receiver BFM.
- Scrambler can be enabled or disabled.
- Supports disparity & invalid code insertion in 8b/10b.
- Supports sync error injection.
- Supports lane skew insertion
- Supports scrambler error injection
- Functional coverage to cover each and every feature of the JESD204 specification
- Testsuite to test each and every feature of JESD204 specification
- Callbacks monitor, transmitter and receiver for various events.
- Status counters for various events on bus.

Benefits

- Faster test bench development and more complete verification of JESD204 designs.

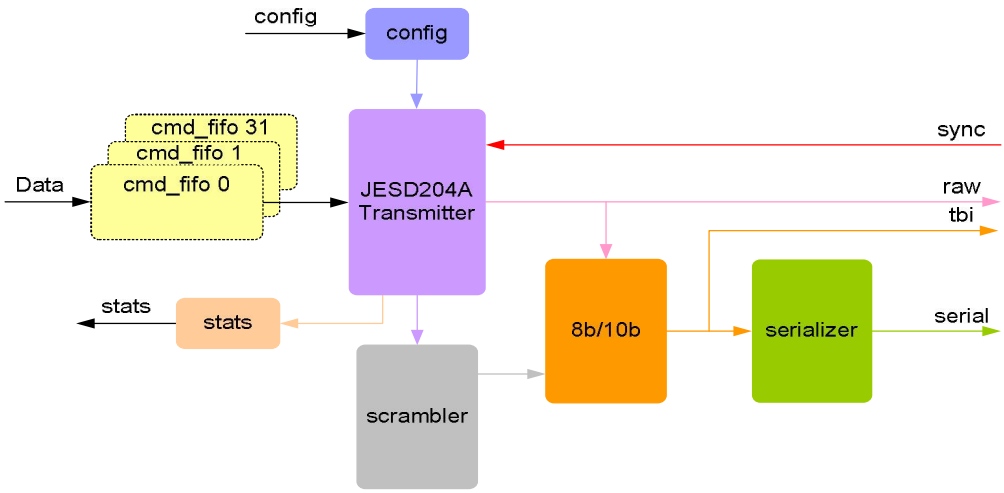
- Simplifies results analysis.
- Runs in every major simulation environment
- Comes with complete test suite to test each and every feature of JESD204.

JESD204 Verification IP Topology



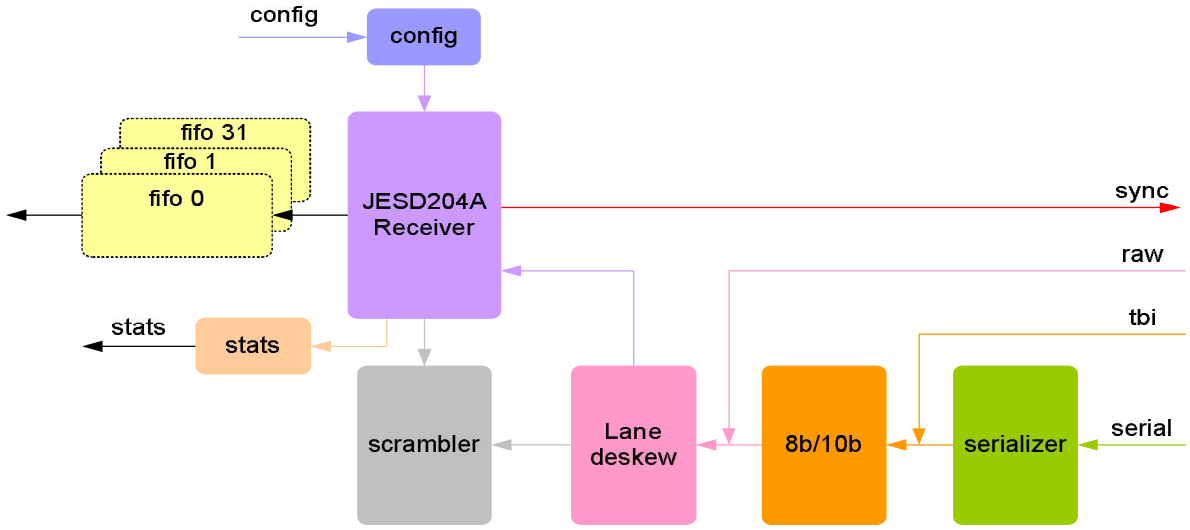
JESD204 BFM Behavior

JESD204 BFM can act as either transmitter or receiver. When acting as Transmitter user need to configuration all the basic configuration parameters like number of convertors, number of lanes and other parameters as per the JESD204 specs. Once configuration is done, user can generated random data to convertors.



User has got access to various generation parameters to fine gain control of error and data generation. At each point of transmission, callbacks are executed to give control to user for modify the default behavior of transmitter or inject error. At end of transmission, transmitter bfm updates the status counter.

When acting as Receiver user need to configuration all the basic configuration parameters like number of convertors, number of lanes and other parameters as per the JESD204 specs. Once configuration is done, Receiver is ready for getting into sync and process the data transmitted by transmitter.



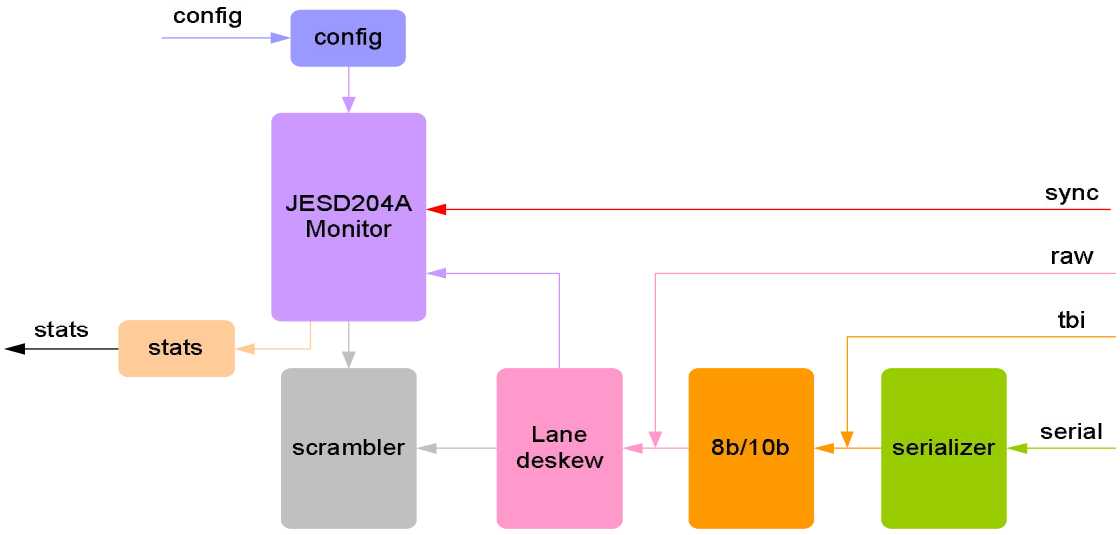
Receiver BFM has ability to assert loss of sync any time user wants and also has ability to detect all possible errors. At end reception, receiver bfm updates the status counter. Like transmitter receiver also implements callbacks for fine grain processing of received events.

JESD204 Monitor Behavior

Monitor is first configured with different configuration parameters. A monitor monitors the bus for protocol errors and timing errors. Monitor also keeps track of all the access on bus, updates the status counters.

Monitor also implements functional coverage, which can be used for tracking quality of verification.

Like transmitter and receiver, monitor implements callbacks.



Supported Simulators

- VCS
- NC-Sim
- ModelSim
- Questasim

Smart DV Technologies India Private Limited,
14/B, 2nd Cross, SR Layout,
Bangalore, Karnataka,
India - 560017
E-Mail : info@smart-dv.com
http://www.smart-dv.com