Smart DV Technologies India Private Limited
14/B, 2nd Cross, SR Layout,
Bangalore, India : 560017
E-Mail : info@smart-dv.com
http://www.smart-dv.com

IEEE 1149.1/1149.6 (JTAG) Verification IP

Datasheet September 2010 – Version 2.0

Overview

The process of verification is getting complex with every passing year; this is due to the fact that complexity of chips is increasing. With such an increasing design complexity, verification tends to consume up to 60-80% project resources and often represents a bottleneck. Having all this in mind, SmartDV has developed number of Verification IP's, which has been created by verification engineers with decades of experience in verifying complex chips.

The SmartDV Verification IP (VIP) for IEEE 1149.1 (JTAG) provides an efficient and simple way to verify and monitor the JTAG controller and collect data on bus. The SmartDV VIP for JTAG Verification IP is fully compliant with JTAG Standard of IEEE 1149.1/1149.6:

- Supports all types of Jtag operations and JTAG Standard of IEEE 1149.1/1149.6 registers.
- Supports all the JTAG connection modes.
- Operates as a Jtag BFM to drive stimulus, protocol checker, Monitor and data collector.

Features

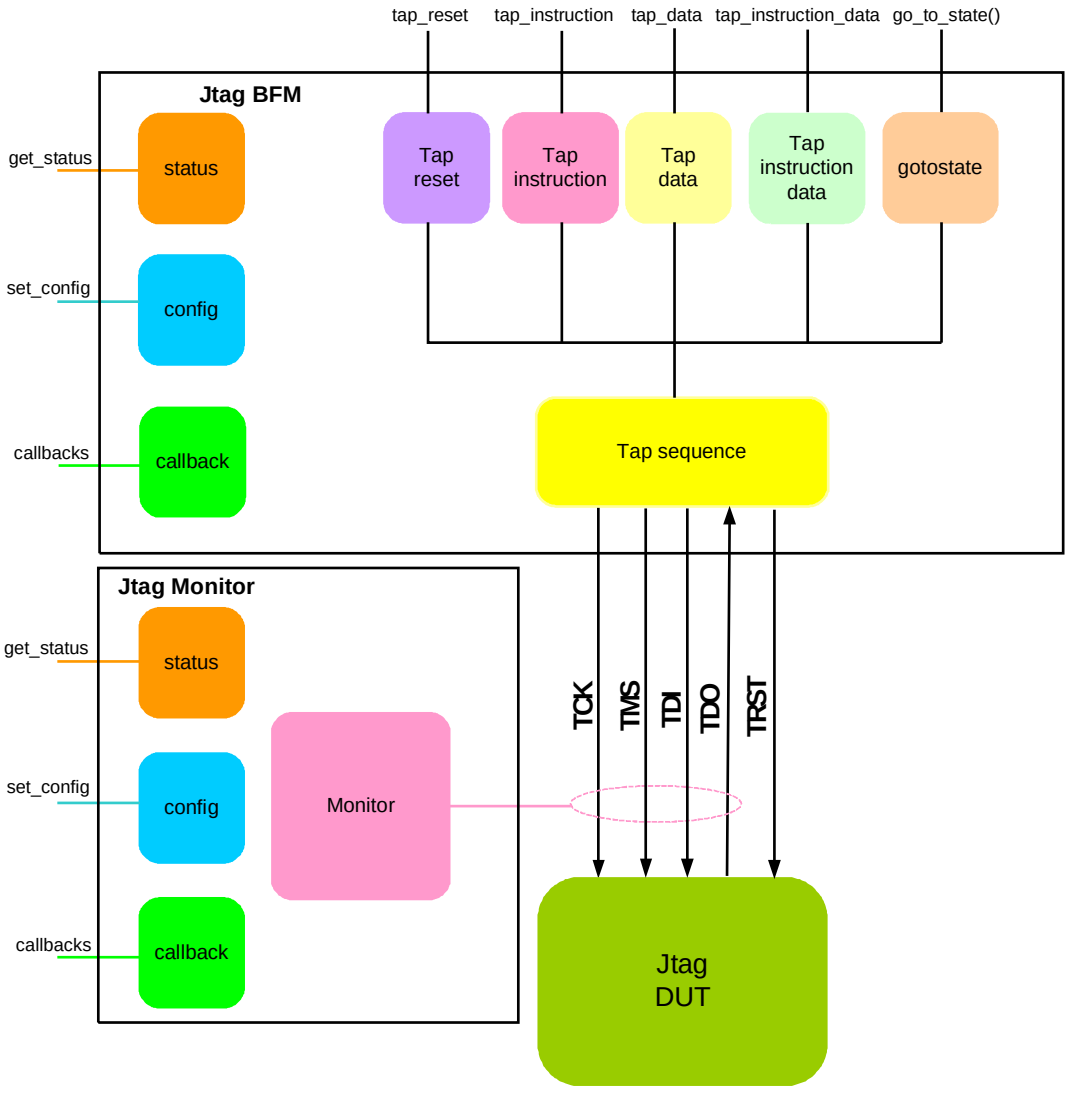
- Implemented in **Unencrypted OpenVera, Verilog, SystemC and SystemVerilog**.
- Supported RVM, AVM, VMM, OVM, UVM and non-standard verify env.
- Supports Jtag protocol standard IEEE 1149.1 and IEEE 1149.6.
- Supports all the JTAG tap instructions.
- Supports programmable clock frequency of operation.
- Checks for following
  - State based rules
  - Active Command rules
  - Read/Write to Instruction and data register Rules.
- Supports Instruction register and data register of size up to 64 bits.
- Proficiency to extend with user defined instructions and registers.
- Proficiency to extend with user defined functional coverage points.
- Has ability to read BSDL file and
  - Automatically generate test vectors to test all BSDL cell types
  - Automatically generate functional coverage points to check if all possible BSDL cell testing is complete

    - Automatically generate SVA assertions properties
- Supports constraints Randomization.
- Status counters for various events on bus.
- Supports callbacks for user to define custom instruction decoder.
- Supports callbacks for user to get callback on each state of TAP controller.
- Support all types of timing and protocol violation detection.
- Notifies the testbench of significant events such as transactions, warnings, timing and Protocol violations.

Benefits

- Faster testbench development and more complete verification of JTAG designs.
- Simplifies results analysis.
- Runs in every major simulation environment.

Jtag Verification IP Topology



Jtag BFM Behavior

JTAG BFM is first configured with different configuration parameters. This is stored in config object in above block diagram. User is provided with rich set of methods to generate a valid instruction to Jtag controller (DUT). Some of the command as shown in above block diagram are tap_reset(), tap_instruction(), tap_data(), tap_instruction_data(), go_to_state().

During execution of above methods, callbacks are executed, where user can override the default behavior of the Jtag BFM or overload the values being driven out. At the end of execution of methods, status counters are updated. User can access this counters anytime during simulation.

User can create complex sequence of commands with help of generic command methods (Not shown in block diagram). Jtag BFM can also be configured to log all the access into a log file, with different debug levels. This can be later used for post processing.

Jtag Monitor Behavior

Monitor is first configured with different configuration parameters; This is stored in config object in above block diagram. After a valid reset, whenever a valid access is detected, monitor collects complete instruction and data associated with command and executes the callback. Also status counters are updated to reflect the current status of the access. Monitor also implements functional coverage, which can be overloaded with user defined functional coverage if there is need.

A monitor monitors the Jtag bus for protocol errors and timing errors. Monitor also keeps track of all the access on bus, and these stats can be accessed any time during simulation.

Jtag monitor can also be configured to log all the access into a log file, with different debug levels. This can be later used for post processing.

Supported Simulators

- VCS
- NC-Sim
- ModelSim
- Questasim
- Aldec Rivera

Smart DV Technologies India Private Limited
14/B, 2nd Cross, SR Layout,
Bangalore, India : 560017
E-Mail : info@smart-dv.com
http://www.smart-dv.com