SmartDV Technologies India Private Limited
14/B, 2nd Cross, SR Layout,
Bangalore, India : 560017
E-Mail : info@smart-dv.com
http://www.smart-dv.com

Microwire Verification IP

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Overview

The process of verification is getting complex with every passing year; this is due to the fact that complexities of chips are increasing. With such an increasing design complexity, verification tends to consume up to 60-80% project resources and often represents a bottleneck. Having all these in mind, SmartDV has developed number of Verification IP's, which has been created by verification engineers with decades of experience in verifying complex chips.

The SmartDV Verification IP (VIP) for Microwire Serial Interface provides an efficient and simple way to verify the Microwire master or slave device. The SmartDV VIP for Micorwire is fully compliant with Microwire Serial interface.

Features

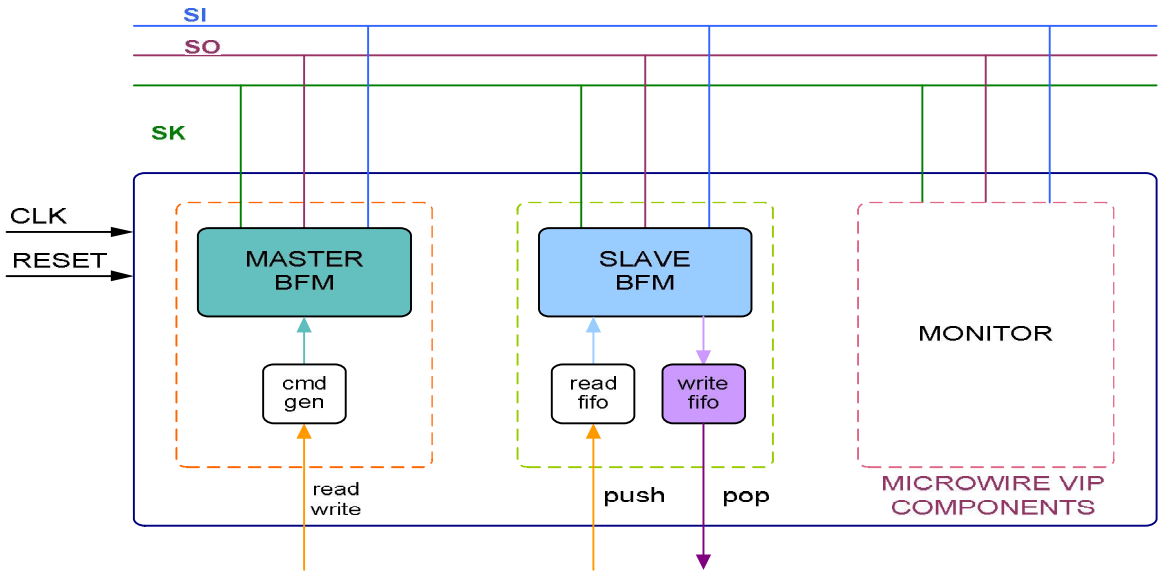
- Implemented in **Unencrypted OpenVera, Verilog, E, SystemC and SystemVerilog**.
- Supported RVM, AVM, VMM, OVM, UVM and non-standard verify env.
- Supports configurable address width from 2 to 32bit.
- Supports configurable data width from 2 to 64bit.
- Support Master and Slave Mode.
- Supports 3-wire interface.
- Support baud rate selection.
- Support internal clock division check.
- Support single and burst transfer mode.
- Support on the fly generation of data.
- Built in functional coverage analysis.
- Supports Callbacks in master, slave and monitor for modifying, and sampling data/cmd on Microwire bus.

Benefits

- Faster testbench development and more complete verification of Microwire designs.

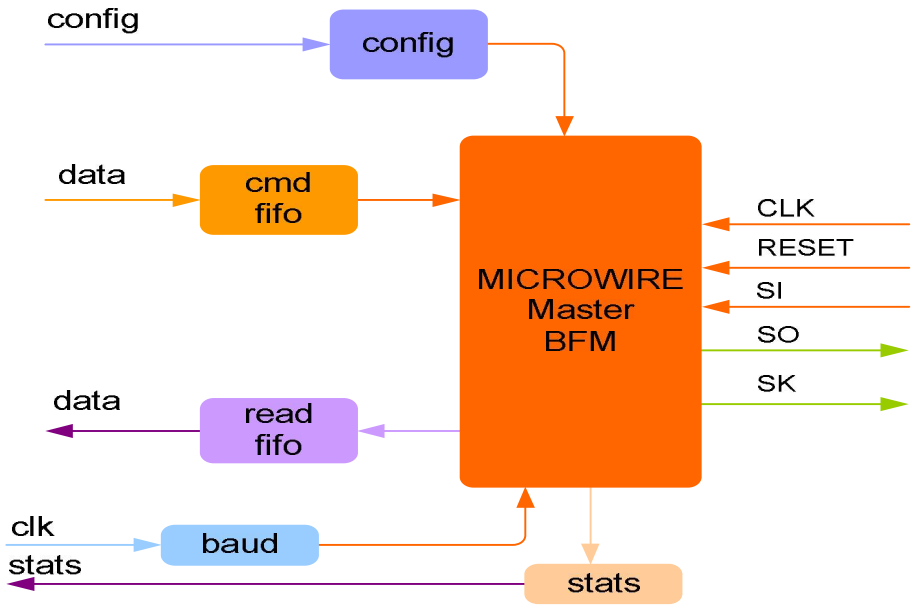
- Easy to use command interface simplifies testbench control and configuration of slave and master.
- Simplifies results analysis.
- Integrates easily into **OpenVera, SytemVerilog, Specman E, and SystemC.**
- Runs in every major simulation environment.

Microwire Verification IP Topology



Master Behavior

Microwire VIP master is first configured with different configuration parameters. Parameters like Baud rate, MSB First.

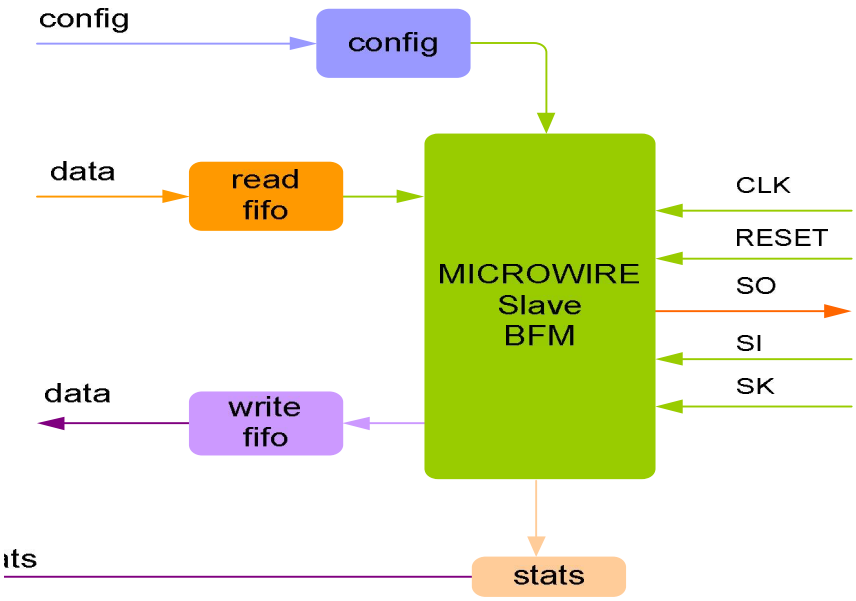


Once configuration is completed, user can use rich set of commands to issue transactions on Microwire bus. When mode is set to FIFO mode, user needs to use command write (data) to write data, read to do read operation, erase to do erase operation. User can use FIFO mode to mimic any kind of master device.

Master BFM supports user callbacks for read and write command processing.

Slave Behavior

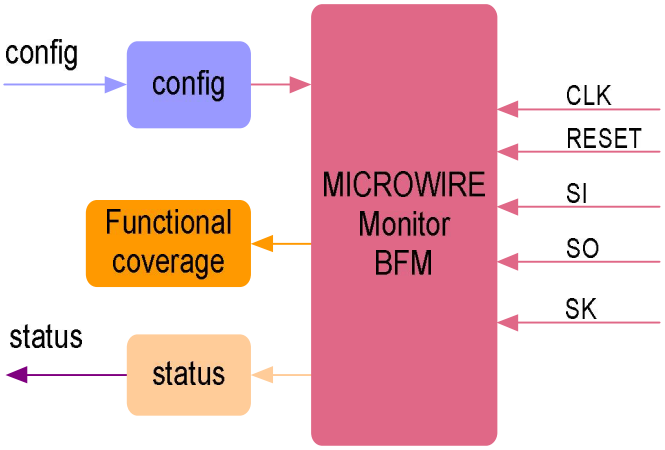
Micorwire VIP slave is first configured with different configuration parameters. Parameters like, Baud rate, MSB First. Once configuration is completed, Microwire VIP slave can respond to transaction on Microwire bus.



Microwire VIP slave device monitors the bus to determine if it has been selected for a transfer request. It will respond to a transfer request if it has been selected. If slave is in FIFO mode, then, slave responds to read requests by sending data which can be fed through its write FIFO. For write requests, the slave receives data transmitted by the master and passes it to the read FIFO. If slave is in Device mode, slave mimics like a device mode it is in. Basically it then uses memory model inside to send out read data or store write data from master.

Monitor Behavior

Monitor is first configured with different configuration parameters. A monitor monitors the Microwire bus for protocol errors and timing errors.



Monitor also keeps track of all the access on bus and these stats can be accessed any time during simulation. Monitor supports user callbacks for read and writes data.

Supported Simulators

- VCS
- NC-SIM
- ModelSim
- Questasim

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