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MIL_STD_1553 Verification IP

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Overview

The process of verification is getting complex with every passing year; this is due to the fact that complexities of chips are increasing. With such an increasing design complexity, verification tends to consume up to 60-80% project resources and often represents a bottleneck. Having all this in mind, SmartDV has developed number of Verification IP's, which has been created by verification engineers with decades of experience in verifying complex chips.

The SmartDV Verification IP (VIP) for MIL_STD_1553B provides an efficient and simple way to verify the MIL_STD_1553B. The SmartDV VIP for MIL_STD_1553B is fully compliant with Standard MIL_STD_1553B Specifications provides the following features:

- The model has a rich set of configuration parameters to control MIL_STD_1553B functionality.
- Ability to detect and insert various types of error.
- The Controller is capable of inserting various transmit errors.
- The receiving is capable of detecting various received errors.

Features

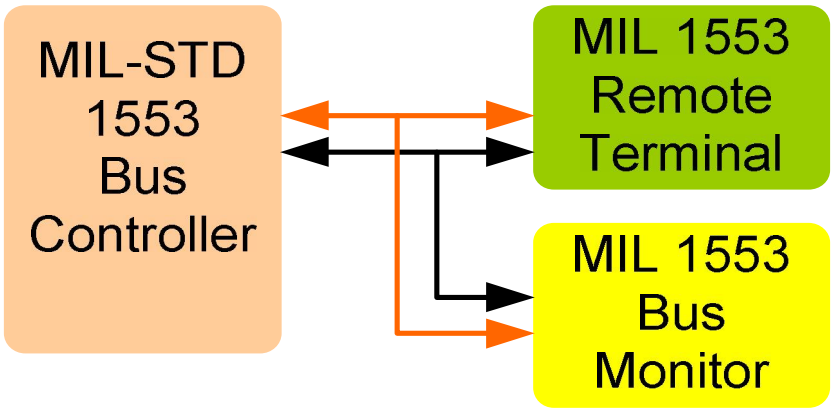
- Implemented in **Unencrypted OpenVera, SystemVerilog, Verilog, SystemC and Specman E.**
- Supported RVM, AVM, VMM, OVM, UVM and non-standard verify env.
- Compliant with MIL-STD-1553B Standard.
- Support Remote terminal, Bus Controller and Bus Monitor.
- Supports configurable length of word length, default 20 bits.
- Supports configurable length of data bits, default 16.
- Supports configurable message length per transfer.
- Supports NRZ and Manchester encoding.
- Supports single or multi bus control.
- Supports following message formats
  - -> Controller to terminal
  - -> Terminal to controller
  - -> Terminal to terminal
  - -> Broadcast
  - -> System control
- Glitch injection and detection

- Supports up to 31 remote terminals
- Supports all types of errors insertion/detection as given below:
  - -> Sync error
  - -> Parity error
  - -> NRZ or Manchester encoding error
  - -> Glitch injection
  - -> Oversize message error
  - -> Undersize message error
  - -> Driving X onto bus
  - -> Various illegal values errors
  - -> Inter message gap error
  - -> Terminal response time error
- Supports test cases from following standards
  - ->MIL-HDBK-1553 Remote Terminal Validation Test Plan Notice 1
  - ->MIL-HDBK-1553A Remote Terminal Validation Test Plan Section 100
  - ->SAE AS-4112 Remote Terminal Production Test Plan
  - ->SAE AS-4113 Bus Controller Validation Test Plan
  - ->SAE AS-4114 Bus Controller Production Test Plan
  - ->SAE AS-4115 Data Bus System Test Plan
  - ->SAE AS-4116 Bus Monitor Test Plan
  - ->SAE AS-4117 Bus Components Test Plan
- On-the-fly protocol and data checking.
- Notifies the test bench of significant events such as transactions, warnings, and protocol violations.
- Status counters for various events on bus.
- Callbacks in Host and Node for various events.
- Built in functional coverage analysis.
- MIL-STD-1553 Verification IP comes with complete test suite to verify each and every feature of MIL-STD-1553B specification.
- FIFO depth programmable.
- Notifies the test bench of significant events such as transactions, warnings, and protocol violations.
- MIL_STD_1553 Verification IP comes with **complete test suite** to verify each and every feature of MIL_STD_1553B specification.
- Built in functional coverage analysis.

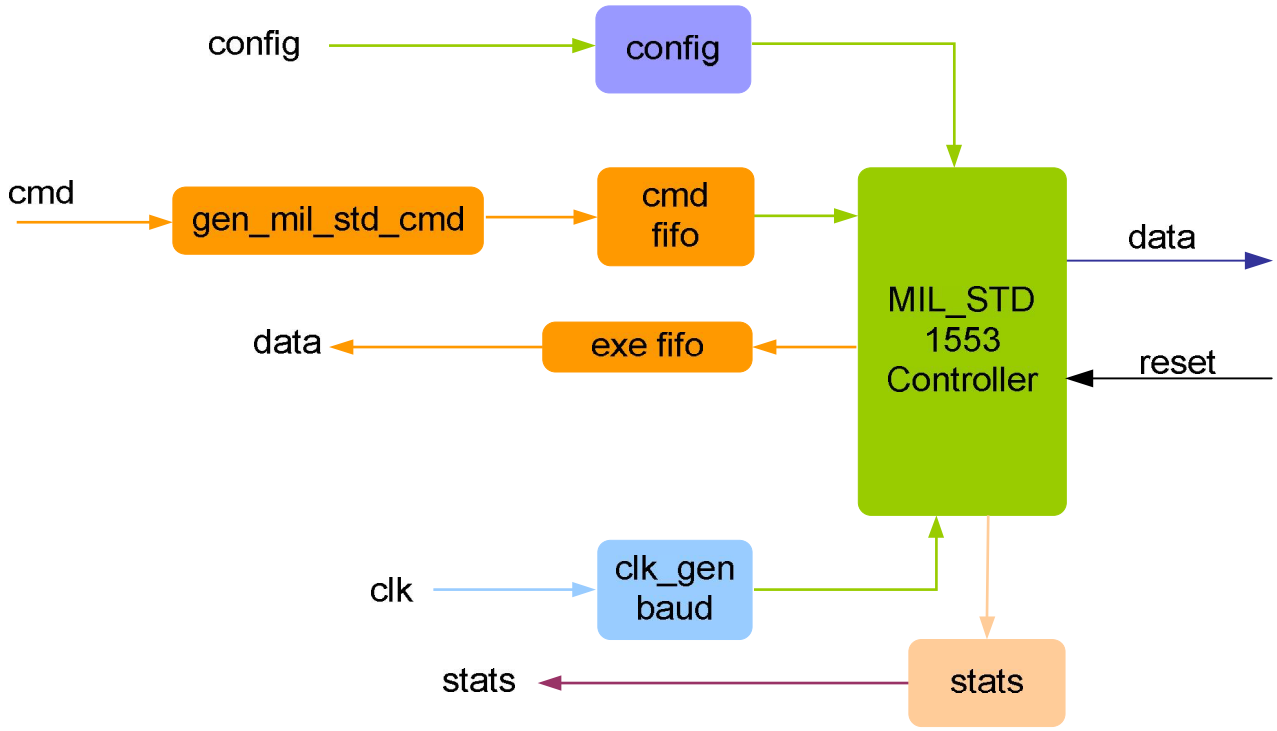
Benefits

- Faster test bench development and more complete verification of MIL_STD_1553 designs.
- Easy to use command interface simplifies test bench control and configuration of Controller and Terminal.
- Simplifies results analysis.
- Runs in every major simulation environment

MIL_STD_1553 Verification IP Topology



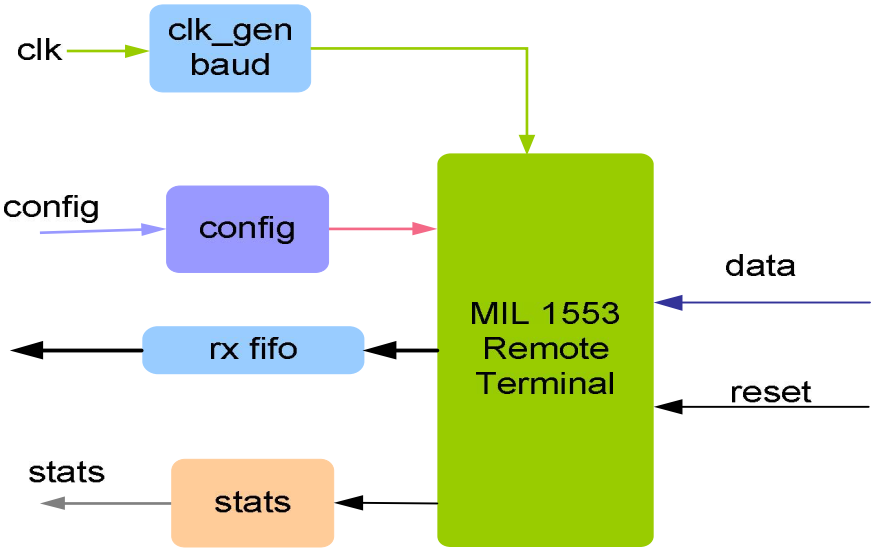
MIL_STD_1553 Controller BFM Behavior



MIL_STD_1553 verification IP acts as a Controller. Controller is first configured with different configuration parameters. Configuration parameters are baud rate, transmit FIFO depth. Error insertion can be performed for common serial data and frame transmission errors. FIFO's are used to store data transmitted during serial.

At each stage of transmission, callbacks are executed for giving control to user to processing the data being transmitted. Status counters are updated at the end of transmission.

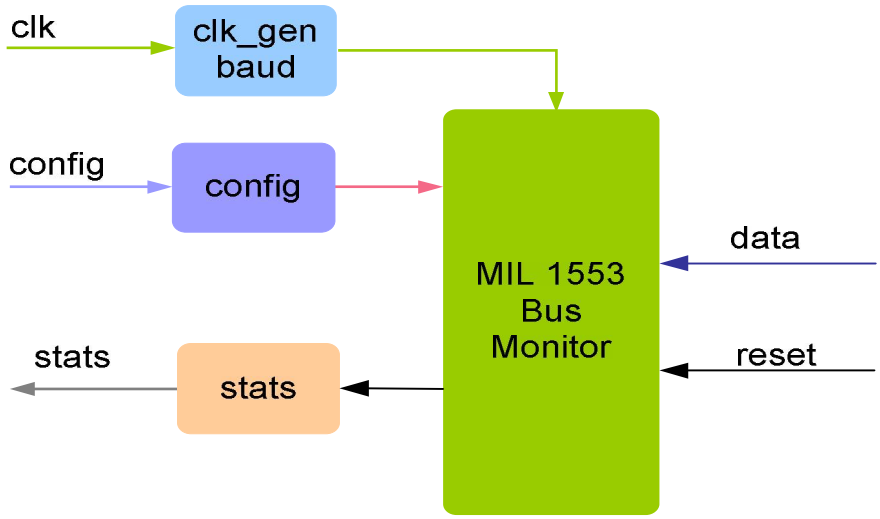
MIL_STD_1553 Terminal BFM Behavior



MIL_STD_1553 verification IP acts as a Terminal. Terminal is first configured with different configuration parameters. Configuration parameters are baud rate, receive FIFO depth. Terminal recovers the clock from serial data, and samples the frames. Error detections is performed for common serial data and frame transmission errors. FIFO's are used to store data received during serial.

At each stage of reception, callbacks are executed for giving control to user to processing the data being transmitted. Status counters are updated at the end of transmission.

Monitor Behavior



Monitor is first configured with different configuration parameters. A monitor monitors the MIL_STD_1553 bus, recovers the clock, and samples frames. Monitor also keeps track of all the access on bus and these stats can be accessed any time during simulation. Protocol checking begins after a valid reset, or without a reset if configured for this condition. The Monitor also logs all transactions into a file that can be configured through the use of log methods.

Supported Simulators

- VCS
- NC-SIM
- Modelsim
- Questasim

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