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MIPI DPHY Verification IP

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Overview

The process of verification is getting complex with every passing year; this is due to the fact that complexities of chips are increasing. With such an increasing design complexity, verification tends to consume up to 60-80% project resources and often represents a bottleneck. Having all this in mind, SmartDV has developed number of Verification IP's, which has been created by verification engineers with decades of experience in verifying complex chips.

The SmartDV Verification IP (VIP) for MIPI DPHY provides an efficient and simple way to verify the MIPI DPHY protocol bus. The SmartDV VIP for MIPI DPHYI is fully compliant with version 1.0 of the MIPI DPHY Bus Specification and provides the following features:

Features

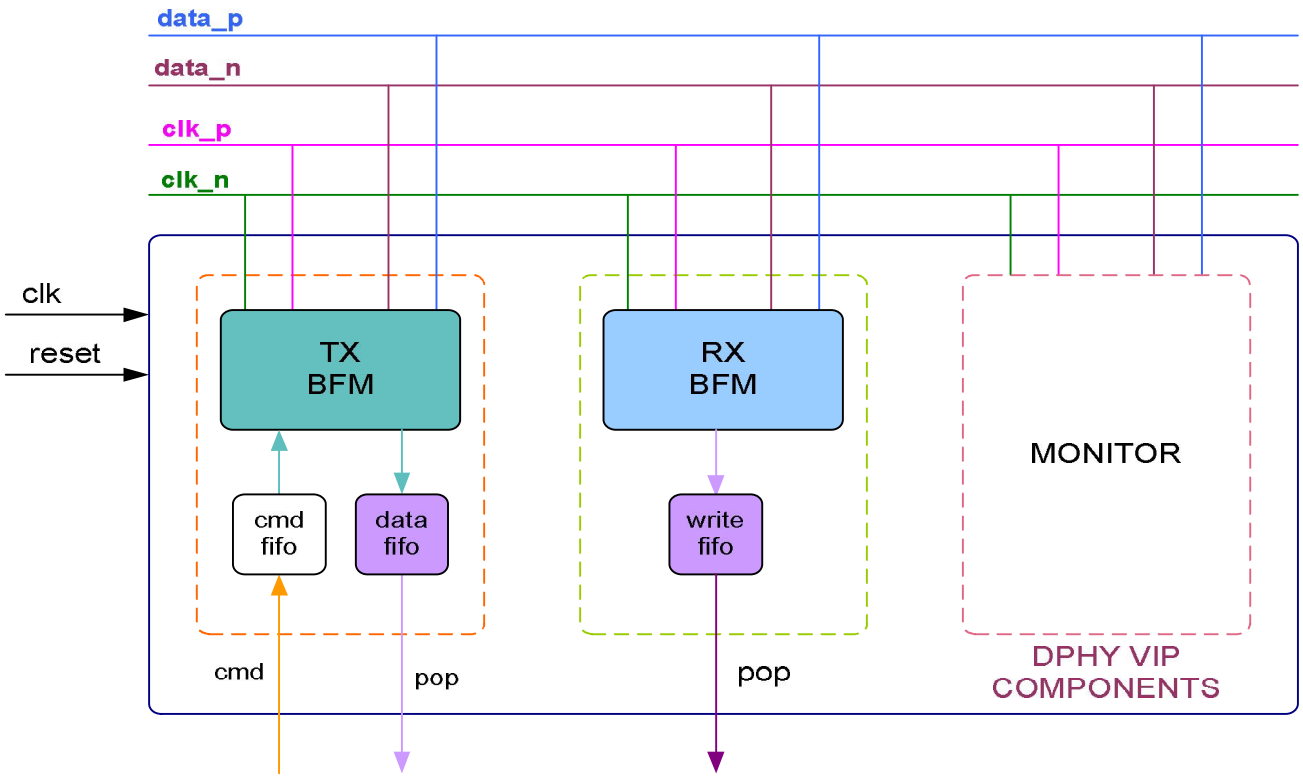
- Implemented in **Unencrypted OpenVera, SystemVerilog, Verilog, SystemC and Specman E.**
- Supported RVM, AVM, VMM, OVM, UVM and non-standard verify env.
- Supports 1.0 MIPI DPHY Specifications.
- Supports both **serial** and **PPI** functionality testing.
- Full MIPI DPHY Transmitter and Receiver functionality.
- Operates as a Transmitter, Receiver
- Monitor, Detects and notifies the test bench of all protocol and timing errors.
- Supports short and long packets
- Supports all types of short packets
- Supports all types of long packets
- Supports BTA testing.
- Supports all lane configuration
- Supports multiple packets per transmission
- Supports differential and single ended mode of operation
- Various kind of Transmitter and Receiver errors generation and detection
  - SoT error
  - Sync error
  - Word count error
  - Sync length error
- Status counters for various events in bus.
- Callbacks in node transmitter, receiver and monitor for user processing of data.

- MIPI DPHY Verification IP comes with **complete test suite** to test every feature of MIPI DPHY specification.
- Functional coverage for complete MIPI DPHY features

Benefits

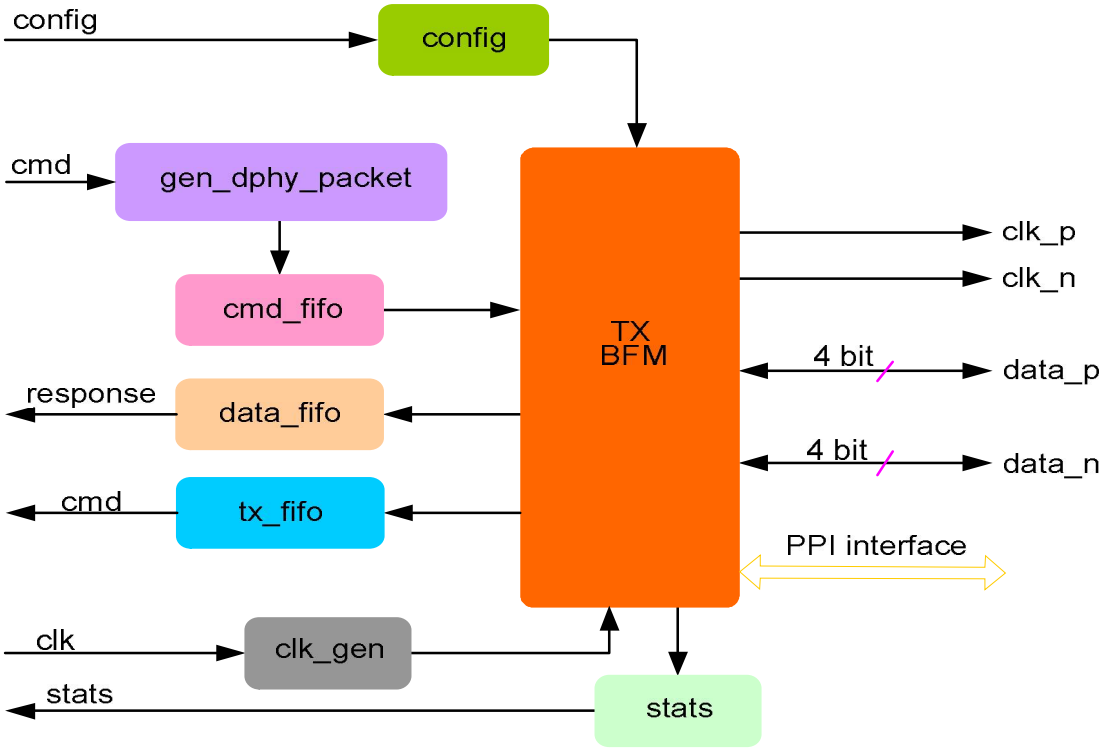
- Faster testbench development and more complete verification of MIPI DPHY designs.
- Simplifies results analysis.
- Integrates easily into **OpenVera, SytemVerilog, Verilog, Specman E, and SystemC**
- Runs in every major simulation environment

MIPI DPHY Verification IP Topology



Transmitter Behavior

MIPI DPHY Tx is first configured with different configuration parameters. MIPI DPHY BFM initiates the possible frames based on the various MIPI DPHY commands from the test bench. User can use the rich set of methods for sending data packets on transmit path of BFM. At each stage of sending data packet, callbacks are executed for giving control to user to processing the packet. Status counters are updated at the end of transmission of frame.

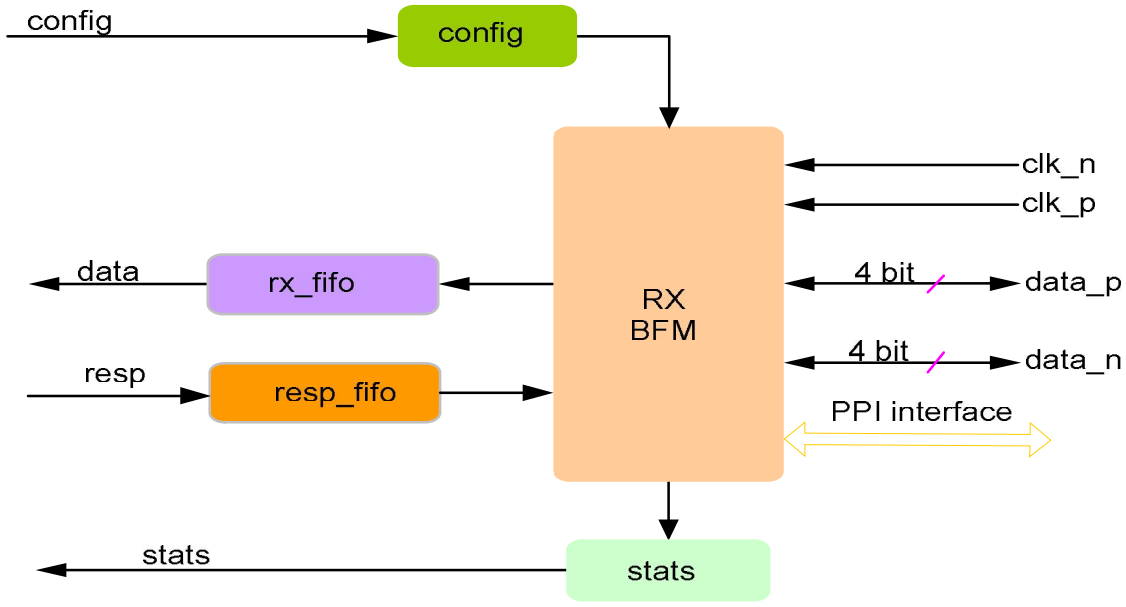


The transmitter can be made to abort in middle of transfer to check if receiver hangs, also transmitter can create various false start and bus idle conditions, insert ecc and checksum errors.

Receiver Behavior

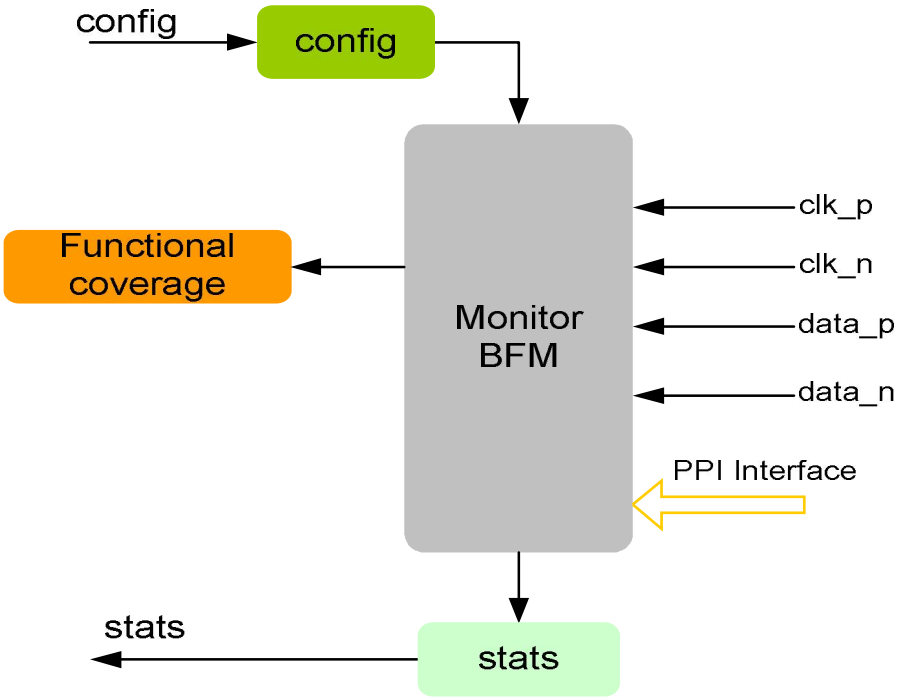
Each receiver is first configured with different configuration parameters. A receiver device monitors the bus and waits for the SoT sequence, once it gets SoT sequence, it collected whole packet and also checks for various types of errors on the bus. Once packet is collected it checks for checksum and ECC errors. In the case of bidirectional mode, Receiver can be controlled to send packets to transmitter, all types like Acknowledge and error report, Acknowledge, Response to read request are supported. Error insertion in response packets can be controller when populating response into response fifo.

The receiver can be made to insert parity errors. Receiver BFM supports user callbacks for read and write command processing.



Monitor Behavior

Monitor is first configured with different configuration parameters. A monitor monitors the MIPI DPHY bus for protocol errors and timing errors.



Monitor also keeps track of all the access on bus, and this stats can be accessed any time during simulation. Monitor implemented callbacks and functional coverage model.

Supported Simulators

- VCS
- NC-Sim
- Modelsim
- Questasim

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