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MIPI SPMI Verification IP

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Overview

The process of verification is getting complex with every passing year; this is due to the fact that complexity of chips are increasing. With such an increasing design complexity, verification tends to consume up to 60-80% project resources and often represents a bottleneck. Having all this in mind, SmartDV has developed number of Verification IP's, which has been created by verification engineers with decades of experience in verifying complex chips.

The SmartDV Verification IP (VIP) for MIPI SPMI provides an efficient and simple way to verify the MIPI SPMI bidirectional two-wire bus. The SmartDV VIP for MIPI SPMI is fully compliant with version 1.0 of the MIPI SPMI Bus Specification and provides the following features:

- Supports full, half speed operations, multi master and multi slave support.
- Operates as a Master, Slave. As a Master, the model can Start/Idle all possible transfers. In addition, as a Slave device it can detect Start/Idle conditions and perform data transfers according to the initiator request.

Features

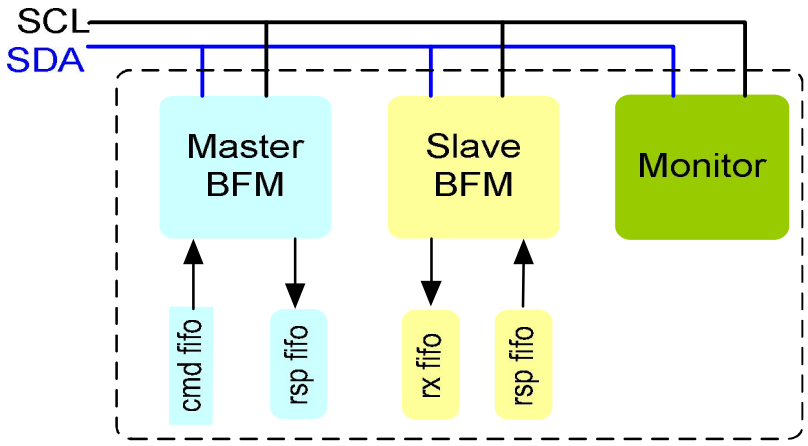
- Implemented in **Unencrypted OpenVera, Verilog, SystemC and SystemVerilog**.
- Supported RVM, AVM, **VMM**, OVM, UVM and non-standard verify env.
- Supports 1.0 MIPI SPMI Specification.
- Full MIPI SPMI Master and Slave functionality.
- Operates as a Master, Slave, or both.
- Monitor, Detects and notifies the testbench of all protocol and timing errors.
- Supports all topologies as per the MIPI SPMI specification
- Supports multiple slaves and masters
- Compares read data with expected results
- Support for slave requests through Alert bit.
- Support for slave request hold.
- Supports following frames
    - Command Frame
    - Data/Address Frame
    - No Response Frame
- Various kind of Master and Slave errors generation
    - Undefined command frame

    - Command frame with parity error
    - Command frame length error
    - Address frame with parity error
    - Data frame with parity error
    - Read of unused register
    - Write of an unused register
    - Read using the broadcast ID or a GSID
- Glitch monitor and injection.
    - Support injection of glitch at all positions of SDATA
    - Support injection of glitch at all positions of SCLK
    - Supports detection of glitches
- Supports extended register read/writes
- Supports device enumeration
- Supports master and slave arbitration
- Bus-accurate timing
- Supports half speed
- Callbacks in master, slave and monitor for various events.
- Status counters for various events in bus.
- Notifies the testbench of significant events such as transactions, warnings, timing and protocol violations.
- Functional coverage of complete MIPI SPMI specs.
- MIPI SPMI Verification IP comes with **complete testsuite** to test every feature of MIPI SPMI specification.

Benefits

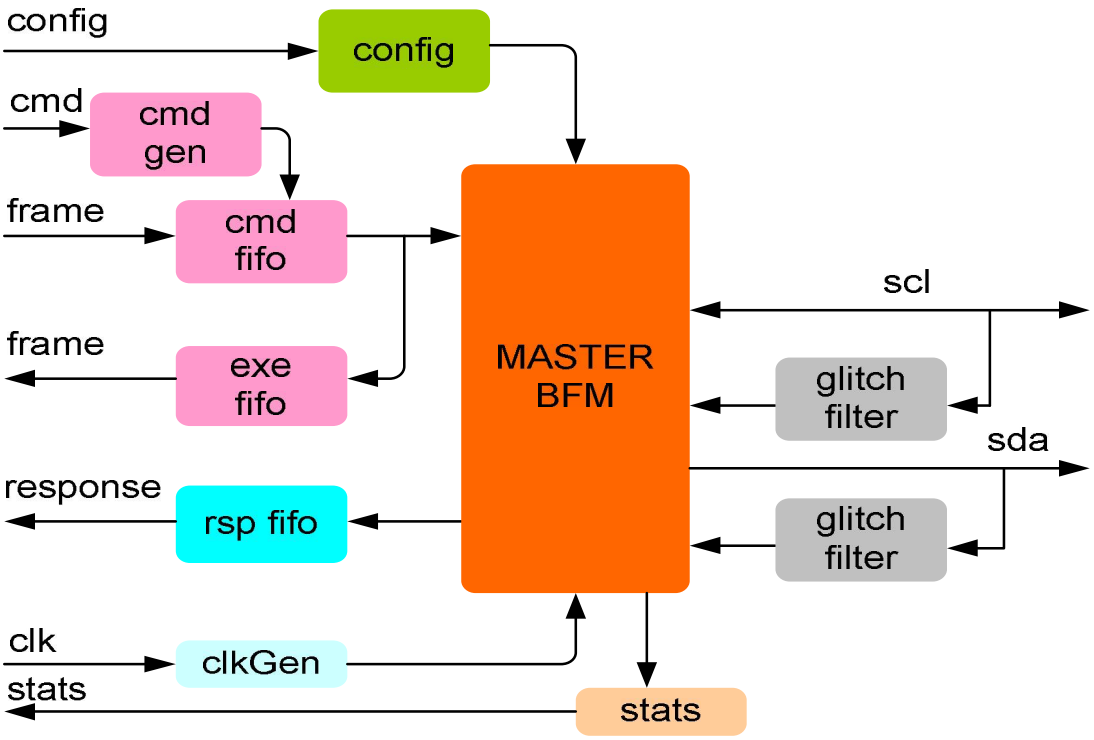
- Faster testbench development and more complete verification of MIPI SPMI designs.
- Simplifies results analysis.
- Integrates easily into **OpenVera, SytemVerilog, Specman E, and SystemC**
- Runs in every major simulation environment

MIPI SPMI Verification IP Topology



Master Behavior

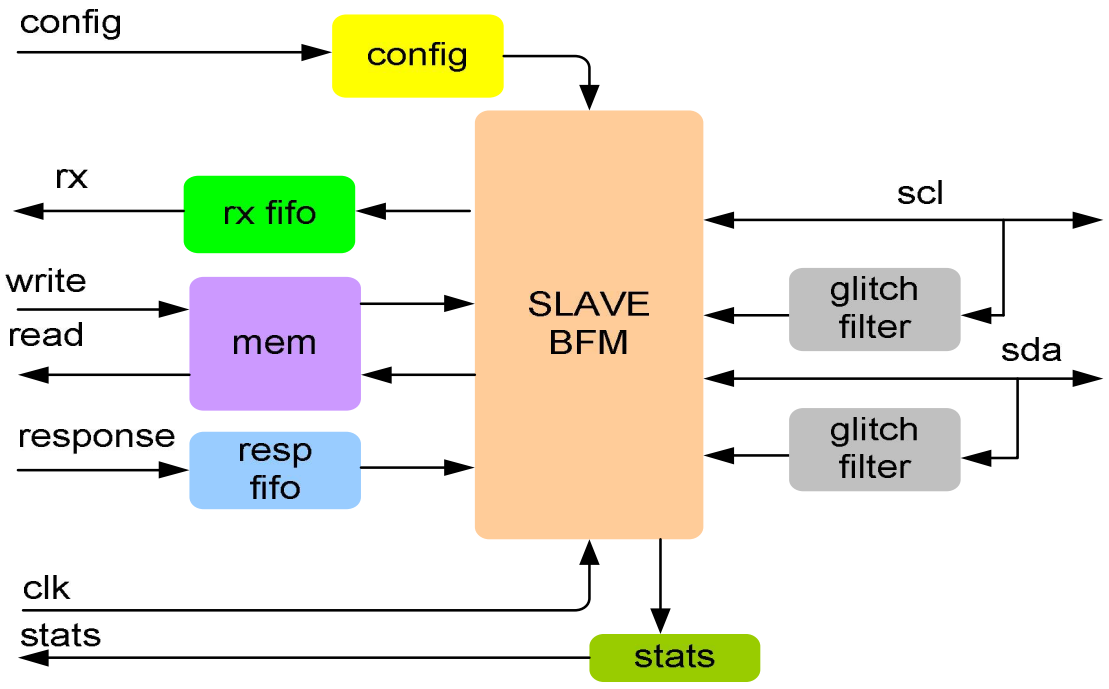
Each master is first configured with different configuration parameters. The master then initiates requests based on frames transfers requests from the testbench. Commands being driven onto bus is pushed into execution fifo. Once processing is done, the command object along with the response in case of read are placed in response fifo



The master can be made to abort in middle of transfer to check if slave hangs, also master can create various false start and bus idle conditions, insert parity errors.

Slave Behavior

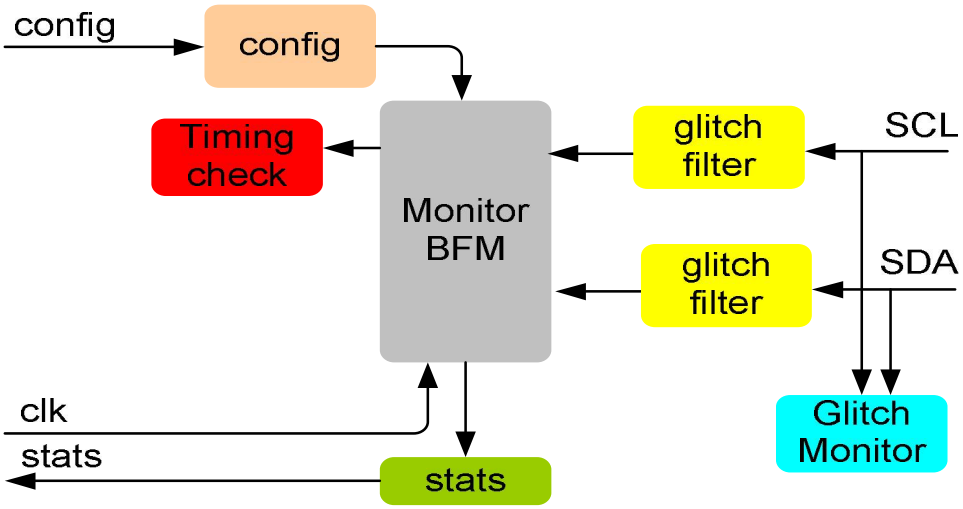
Each slave is first configured with different configuration parameters. A slave device monitors the bus to determine if it has been selected for a transfer request. It will always respond to a transfer request if it has been selected. The salve can be configured to respond either from internal memory model or from responses in response fifo. All the frames targeted to current slave are pushed into rx fifo.



The slave can be made to insert parity errors. Slave BFM supports user callbacks for read and write command processing.

Monitor Behavior

Monitor is first configured with different configuration parameters. A monitor monitors the MIPI SPMI bus for protocol errors and timing errors.



Monitor also keeps track of all the access on bus, and this stats can be accessed any time during simulation. Monitor implemented callbacks and functional coverage model.

Supported Simulators

- VCS
- NC-Sim
- Modelsim
- Questasim

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