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MIPI UniPro Verification IP

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Overview

The process of verification is getting complex with every passing year; this is due to the fact that complexity of chips is increasing. With such an increasing design complexity, verification tends to consume up to 60-80% project resources and often represents a bottleneck. Having all this in mind, SmartDV has developed number of Verification IP's, which has been created by verification engineers with decades of experience in verifying complex chips.

The SmartDV Verification IP (VIP) for MIPI UniPro provides an efficient and simple way to verify and monitor the MIPI UniPro and collect data on bus. The SmartDV VIP for MIPI UniPro Verification IP is fully compliant with MIPI UniPro Specification 1.10, 1.40 and 1.41.

- Supports all types of MIPI UniPro layers
- Operates as UniPro BFM, and MONITOR
- Phy layer is based on D-PHY and M-PHY

Features

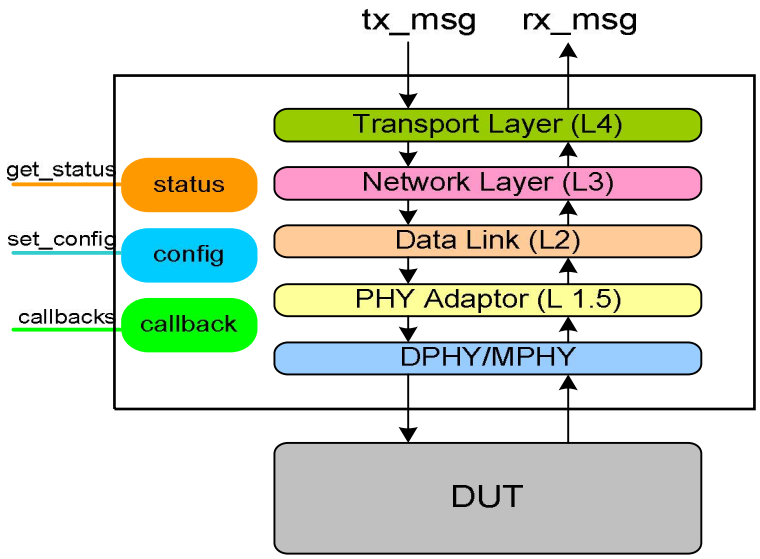
- Implemented in **Unencrypted OpenVera, Verilog, E, SystemC and SystemVerilog**.
- Supported RVM, AVM, **VMM**, OVM, UVM and non-standard verify env.
- Supports MIPI UniPro specification 1.10, 1.40 and 1.41
- Supports MIPI DPHY Specification 1.0
- Support MIPI MPHY specification 1.0
- Supports data control at each layer of UniPro Specification for easy debug.
- Supports multiple connections in L4 Layer and L4 segments
- Support all valid segment sizes in L4 Layer
- Supports invalid field value insertion and detection in L4 Layer
- Supports end to end flow control at L4 layer
- Supports Cport arbitration at both segment level and packet level.
- Supports Layer 3 error injection and detection
- Supports L2 data frames and control frames
- Supports injection of Errors and detection of errors in L2 data frames and control frames.
- Support preemption and preemption error injection for L2 data frames
- Phy layer supports MPHY serial, MPHY RMMI (10,20,40 bit) Interface
- Phy layer supports multi lanes, Type-I and all power modes for Mphy
- Support error injection of all PACP frames.

- Supports link startup as per specs
- Support fine grain control and when flow control needs to be done and how to respond to flow control.
- Supports callbacks for user to get packets or errors in transmitter and receiver and monitor.
- MIPI UniPro verification IP comes with complete testsuite to test every feature of MIPI UniPro spec.
- Functional coverage for each functional condition in env.
- Notifies the testbench of significant events such as transactions, warnings, timing and protocols violations.

Benefits

- Faster testbench development and more complete verification of MIPI UniPro Designs
- Easy to use command interface simplifies testbench control and configuration of slave and master.
- Simplifies results analysis.
- Integrates easily into **OpenVera, SytemVerilog, Specman E, and SystemC**
- Runs in every major simulation environment

MIPI UniPro Verification IP Topology



MIPI UniPro BFM Behavior

MIPI UniPro BFM is first configured with different configuration parameters; SmartDV's MIPI UniPro verification supports rich set of configuration parameters to control each and every possible configuration parameter. This is stored in config object in above block diagram. User is provided with rich set of methods to generate different types of packets/messages/frames on the MIPI UniPro physical interface. User has access to advance error insertion methods,

which allow user to insert errors in any layer, like inserting CRC error logical layer or inserting errors in PHY layer.

MIPI UniPro receiver receives various packets/messages/frames based on the user response programming, it responds after certain delay, and errors responses.
MIPI UniPro receiver has the capability to detect various error like invalid field values, invalid timing in PHY layer, CRC errors. Receiver supports user controlled flow control packet generator or buffer depth based flow control generation.

During execution of above methods, callbacks are executed, where user can override the default behavior of the MIPI UniPro BFM. At the end of execution of methods, status counters are updated. User can access this counters anytime during simulation.

User can create complex sequence of commands with help of generic command methods (Not shown in block diagram). MIPI UniPro BFM can also be configured to log all the access into a log file, with different debug levels. This can be later used for post processing.

MIPI UniPro Monitor Behavior

Monitor is first configured with different configuration parameters. This is stored in config object in above block diagram. After a valid reset, whenever a valid access is detected, monitor collects complete packet and data associated with command and executes the callback. Also status counters are updated to reflect the current status of the access.

A monitor monitors the MIPI UniPro bus for protocol errors and timing errors. Monitor also keeps track of all the access on bus and these stats can be accessed any time during simulation. MIPI UniPro monitor can also be configured to log all the access into a log file, with different debug levels. This can be later used for post processing. Monitor implements functional coverage.

Supported Simulators

- VCS
- NC-Sim
- ModelSim
- Questasim

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