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MIPI MPHY Verification IP

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Overview

The process of verification is getting complex with every passing year; this is due to the fact that complexities of chips are increasing. With such an increasing design complexity, verification tends to consume up to 60-80% project resources and often represents a bottleneck. Having all this in mind, SmartDV has developed number of Verification IP's, which has been created by verification engineers with decades of experience in verifying complex chips.

The SmartDV Verification IP (VIP) for MIPI MPHY provides an efficient and simple way to verify the MIPI MPHY. The SmartDV VIP for MIPI MPHY is fully compliant with MIPI MPHY 1.0 Specification and provides the following features:

- The model supports key features of MIPI MPHY 1.0 including Type 1 and Type II.
- The model has a rich set of configuration parameters to control MIPI MPHY functionality.

Features

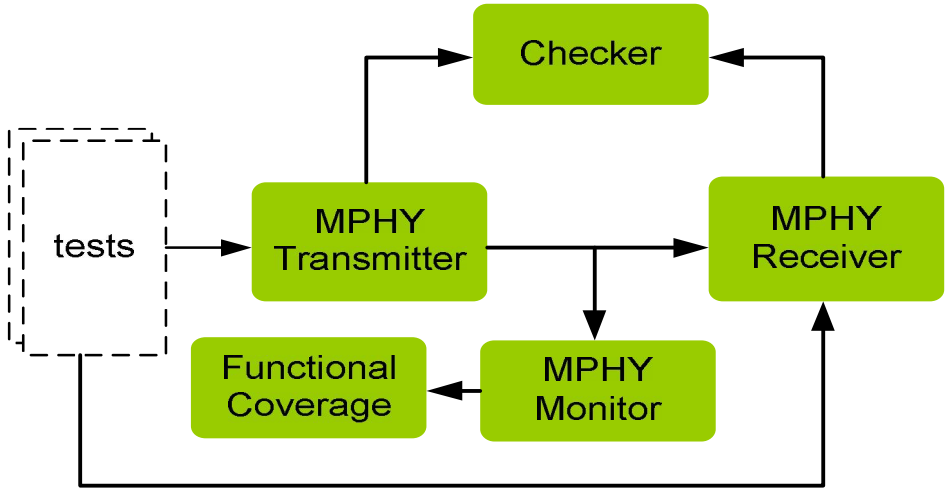
- Implemented in **Unencrypted OpenVera, SystemVerilog, Verilog, SystemC and Specman E.**
- Supported RVM, AVM, VMM, OVM, UVM and non-standard verify env.
- Supports 1.0 MIPI MPHY Specification.
- Support Type-1 and Type-II operations
- Supports both serial and protocol layer interface
- Supports all PWM 0-7 gear of operation
- Supports all HS 1-2 gear of operation
- Supports disabling of NRZ and PWM for easy serial debugging
- Support fine grain control of each timing parameter
- Support timing checks to validate each timing period
- Support programmable sync pattern and length
- Support following 8b/10b error insertion and detection
  - Invalid K character injection
  - Injection of disparity errors
  - Wrong K character injection
  - Corruption of Marker characters
- Supports periodic Filler (NOP) insertion
- Supports periodic Marker 1 insertion

- Support Line configuration
- Support inband reset signaling and detection
- Monitor, Detects and notifies the testbench of all protocol and timing errors.
- Supports constraints Randomization.
- Status counters for various events in bus.
- Callbacks in transmitter and receiver for various events.
- MIPI MPHY Verification IP comes with complete test suite to test every feature of MIPI MPHY specification.
- Functional coverage for complete MIPI MPHY features

Benefits

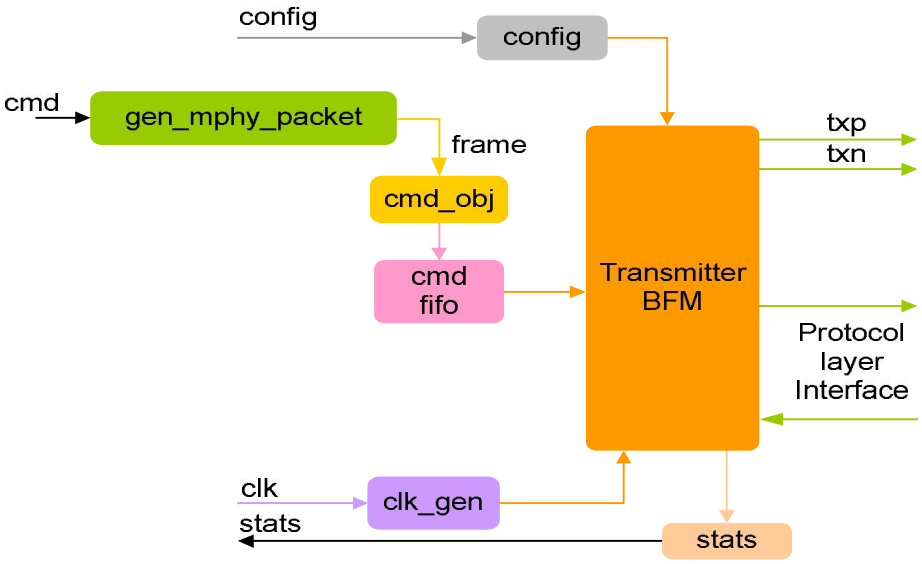
- Faster testbench development and more complete verification of MIPI MPHY designs.
- Simplifies results analysis.
- Integrates easily into OpenVera, SystemVerilog, Verilog, SystemC, Specman E
- Runs in every major simulation environment

MIPI MPHY Verification IP Topology



Transmitter Behavior

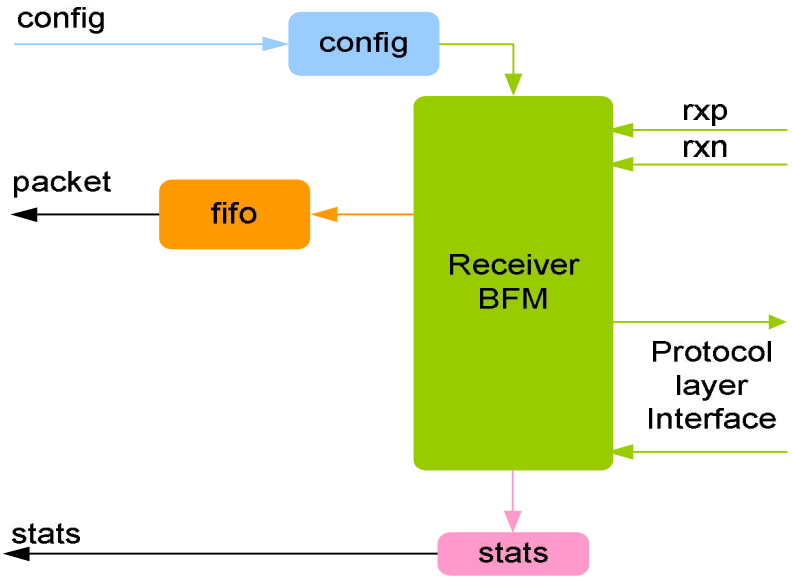
MIPI MPHY transmitter is first configured with different configuration parameters. The transmitter then initiates requests based commands from the testcases. Transmitter supports mixing low speed and high speed commands in same simulation. Supports injection of various 8b/10b errors, timing violations. At the end of transmitting each packet transmission stats are updated.



At each stage of the MPHY transmit FSM, callbacks are executed and user can use this callbacks to modify the behavior of the transmit FSM.

Receiver Behavior

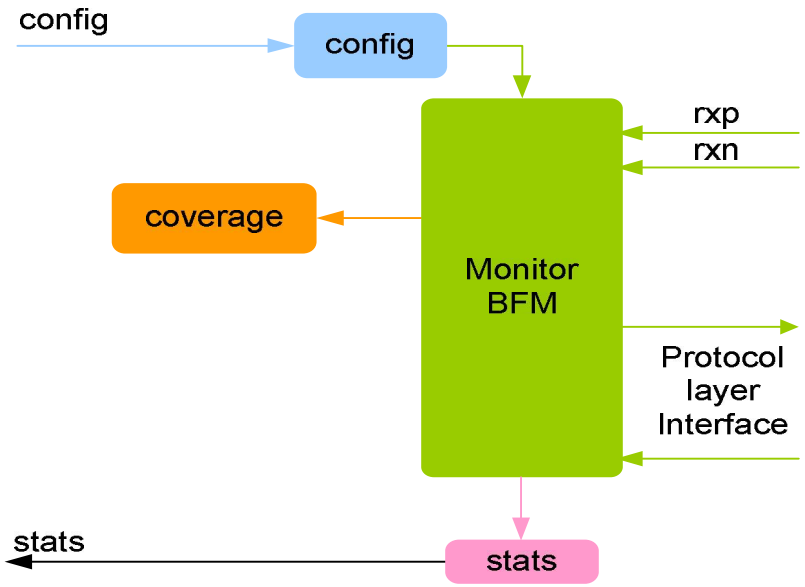
Each receiver is first configured with different configuration parameters. Receiver monitors rxp and rxn pins to make various state machine transitions, it recovers the clocks, converts the serial data to parallel data, locks on to correct 10 bit data and decodes into 8 bit for processing by the state machine.



At each stage of the MPHY receive FSM, callbacks are executed and user can use this callbacks to modify the behavior of the receive FSM.

Monitor Behavior

Monitor is first configured with different configuration parameters. A monitor monitors the bus for protocol errors and timing errors. Monitor also keeps track of all the accesses on bus and these stats can be accessed any time during simulation. The Monitor also logs all transactions into a file that can be configured through the use of methods. The monitor implements the functional coverage per lane.



Supported Simulators

- VCS
- NC-SIM
- Modelsim
- Questasim

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