

NFCIP-1 Verification IP

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Overview

The process of verification is getting complex with every passing year; this is due to the fact that complexities of chips are increasing. With such an increasing design complexity, verification tends to consume up to 60-80% project resources and often represents a bottleneck. Having all this in mind, SmartDV has developed number of Verification IP's, which has been created by verification engineers with decades of experience in verifying complex chips.

The SmartDV Verification IP (VIP) for NFC provides an efficient and simple way to verify the Near Field Communication, which is simple wireless communication between the close coupled devices. The SmartDV VIP for ISO/IEC18092/14443 is fully compliant with standard ECMA-340 Specification and provides the following features:

Features

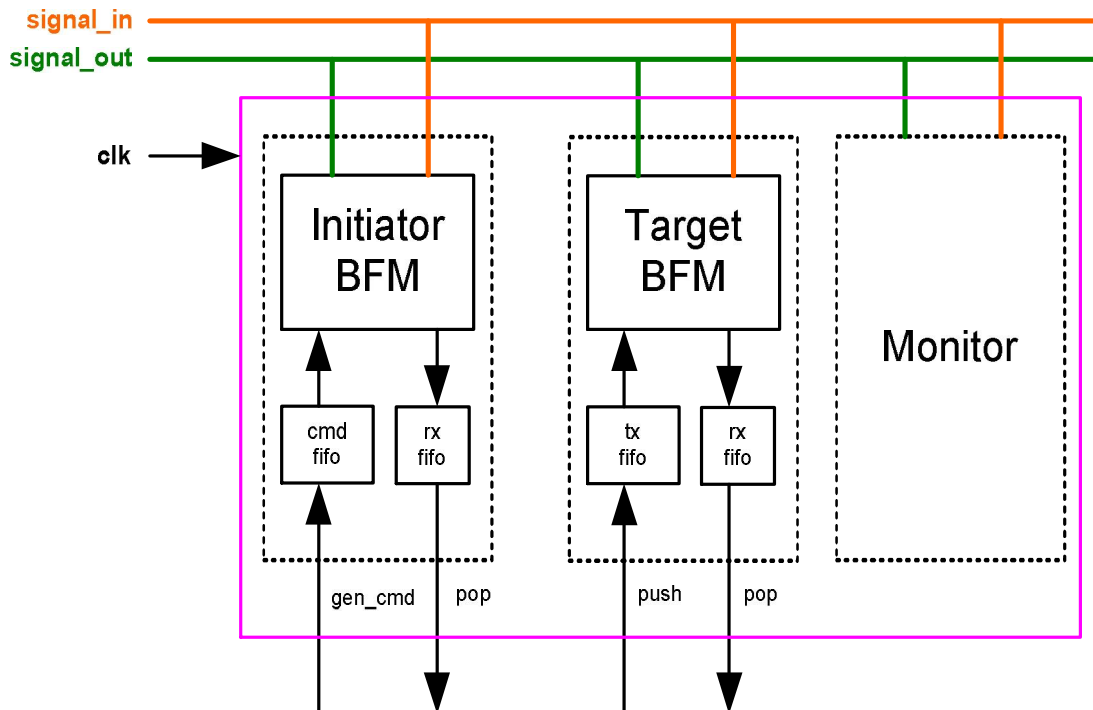
- Implemented in **Unencrypted OpenVera, SystemVerilog, Verilog, SystemC and Specman E.**
- Supported RVM, AVM, VMM, OVM, UVM and non-standard verify env.
- Complete ISO/IEC18092/14443 Initiator/Target functionality.
- Support Half Duplex of operations.
- Supports all the three data rates.
 - 106 kbps
 - 212 kbps
 - 424 kbps
- Supports two different kinds of communication modes.
 - Active communication mode
 - Passive communication mode
- Supports the Multi Activation feature, which allows the Initiator to hold several Targets active simultaneously.
- Supports the chaining feature, which allows the Initiator or Target to transmit information that does not fit in a single block, by dividing the information into several blocks.
- Supports the following types of error insertion and detection.
 - Sync error
 - DID error
 - Length error
 - Acknowledgement error

- Invalid command error
- CRC error
- Parity error
- Re-transmission of corrupted messages.
- Supports to change the parameters(Transfer speed and Frame length) of Initiator and Target after the activation.
- Monitors, detects and notifies the testbench of significant events such as transactions, warnings, timing and protocol violations.
- Status counters for various events on bus.
- NFC Verification IP comes with complete test suite to test every feature of NFC specification.
- Callbacks in initiator, target and monitor for user processing of data.
- Supports constraints Randomization.
- Functional coverage for complete NFC features.

Benefits

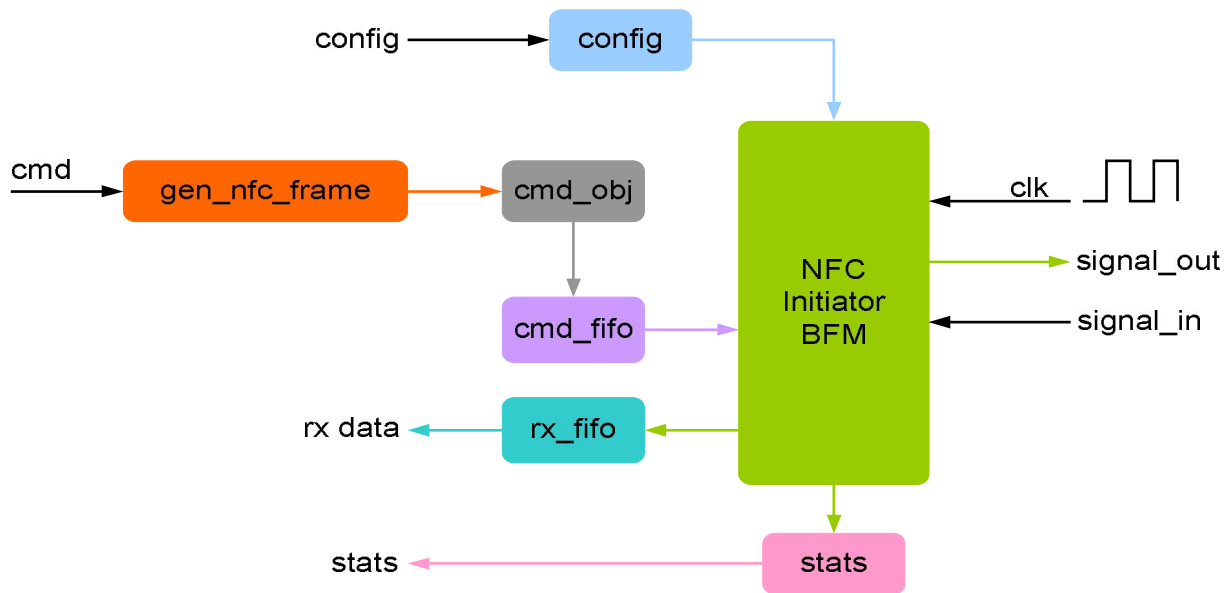
- Faster testbench development and more complete verification of NFC designs.
- Simplifies results analysis.
- Integrates easily into **OpenVera, SytemVerilog, Verilog, Specman E, and SystemC.**
- Runs in every major simulation environment.

NFCIP-1 Verification IP Topology



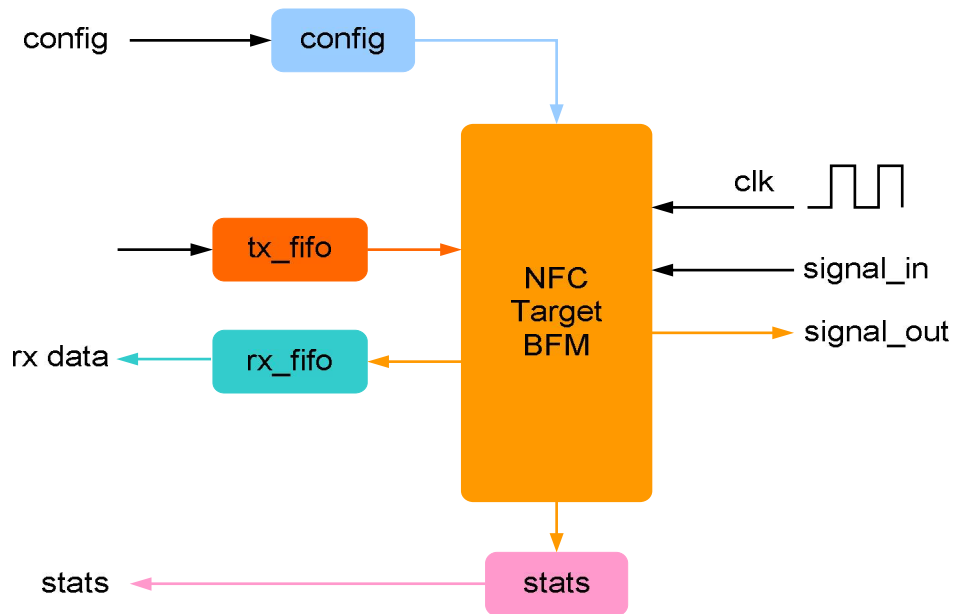
Initiator Behavior

NFC Initiator is first configured with different configuration parameters. NFC BFM initiates the possible requests based on the various NFC commands from the testbench. User uses the rich set of methods for sending frames on Tx path of BFM. At each stage of sending frame, callbacks are executed for giving control to user to processing the frame. Status counters are updated at the end of transmission of frame.



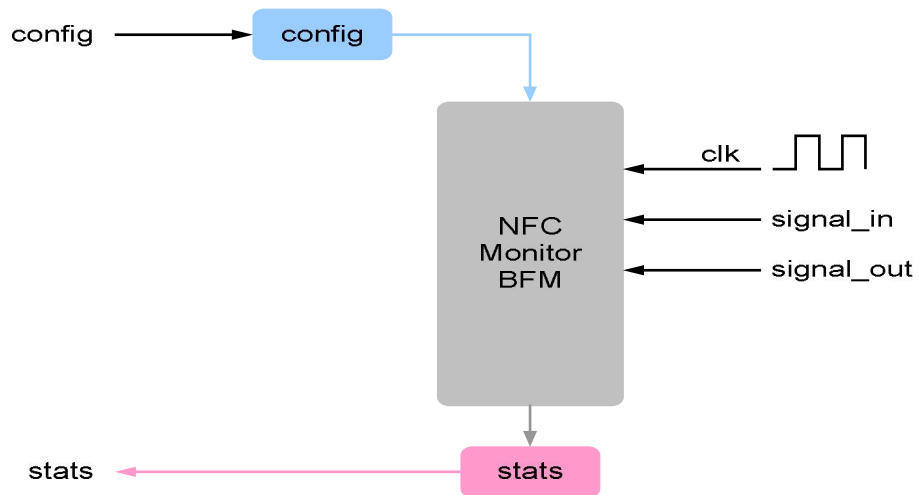
Target Behavior

NFC Target is first configured with different configuration parameters. A target device monitors the bus to determine if it has been selected for a transfer request. It will always respond to a transfer request if it has been selected. The read data on the Rx path of target is collected in the Rx FIFO. At each stage of frame collections, callbacks are used for give control to the user to process the frame. At the end of frame reception, status counters are updated.



Monitor Behavior

Monitor is first configured with different configuration parameters. A monitor monitors the NFC bus for protocol errors and timing errors. Monitor also keeps track of all the accesses on bus, updates the status counters. These statuses can be accessed any time during simulation.



Supported Simulators

- VCS
- NC-SIM
- ModelSim
- Questasim

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