Smart DV Technologies India Private Limited
14/B, 2nd Cross, SR Layout,
Bangalore, India : 560017
E-Mail : info@smart-dv.com
http://www.smart-dv.com

PCI Express Verification IP

Datasheet April 2012 – Version 1.0

Overview

The process of verification is getting complex with every passing year; this is due to the fact that complexity of chips are increasing. With such an increasing design complexity, verification tends to consume up to 60-80% project resources and often represents a bottleneck. Having all this in mind, SmartDV has developed number of Verification IP's, which has been created by verification engineers with decades of experience in verifying complex chips.

The SmartDV Verification IP (VIP) for PCIE provides an efficient and simple way to verify the PCIE 1.0/2.0/3.0 protocol bus. The SmartDV VIP for PCIE is fully compliant with PCI Express Revision 3.0 Specification and provides the following features:

- Supports full PCI Express specification.
- Operates as PCIE Root Complex, PCIE Endpoint and PCIE Monitor.

Features

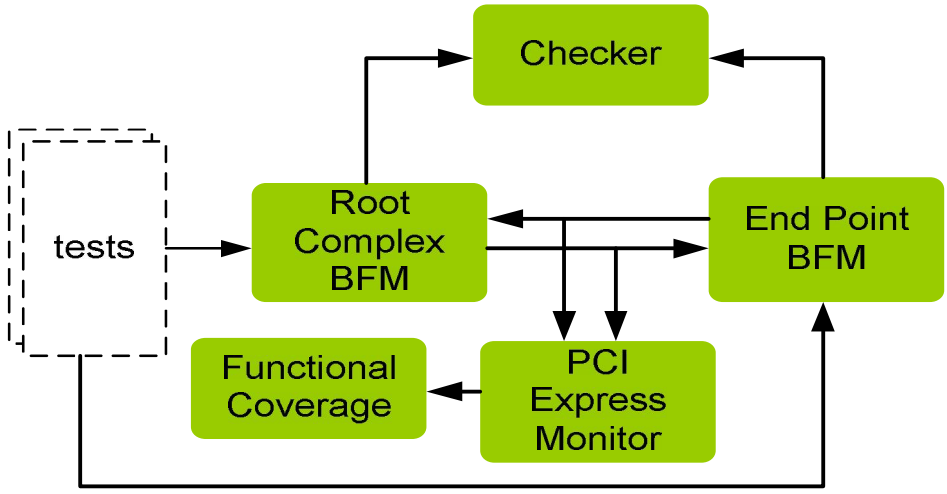
- Implemented in **Unencrypted OpenVera, Verilog, SystemC and SystemVerilog**.
- Supported RVM, AVM, **VMM**, **OVM**, **UVM** and non-standard verify env.
- Supports PCIE Express specs 1.0/2.0/3.0
- Supports PIPE, PCS/PMA, and serdes interface.
- UVM and Verilog APIs supplied, as well as C DPI exports
- Support for Gen 1, 2 and 3, including SSC
- Full link speed and width negotiation up to 32 Lanes
- Automated Error Injections at all layers
- Checkers verify protocol timing checks and functional accuracy at each layer
- Queuing for 8 VCs with configurable depth
- Configurable TC to VC queue mapping
- Support for multiple Requestor / Completer applications, including user supplied applications
- User interface for direct TLP queuing and receipt
- Checks all TLPs for correct formation of headers, prefixes, and ECRC
- Full DL state machines
- Checks all framing, LCRC, and lane rules
- Check all DLLP fields and formatting
- Interface to send / receive user defined DLLPs
- Supports ASPM and Software controlled Power Management

- Automated Error Injections and checking
- Full LTSSM state machine
- SERDES model with digital clock recovery
- Speed and Link Width negotiation
- Supports Upconfigure, polarity inversion, and lane-to-lane skew
- Configurable Spread Spectrum Clocking (SSC)
- Gen 1 & 2 PCS, 8b/10b encoding
- Gen 3 128/130 encoding
- Configurable timers and timeouts
- Callbacks in Host, Device and monitor for user processing of data
- Notifies the testbench of significant events such as transactions, warnings, timing and protocol violations.
- PCI Express Verification IP comes with **complete testsuite** to test every feature of PCI Express specification**.**
- Functional coverage for complete PCI Express features.

Benefits

- Faster testbench development and more complete verification of PCI Express designs.
- Simplifies results analysis.
- Integrates easily into **OpenVera, SytemVerilog,SystemC,Verilog**
- Runs in every major simulation environment

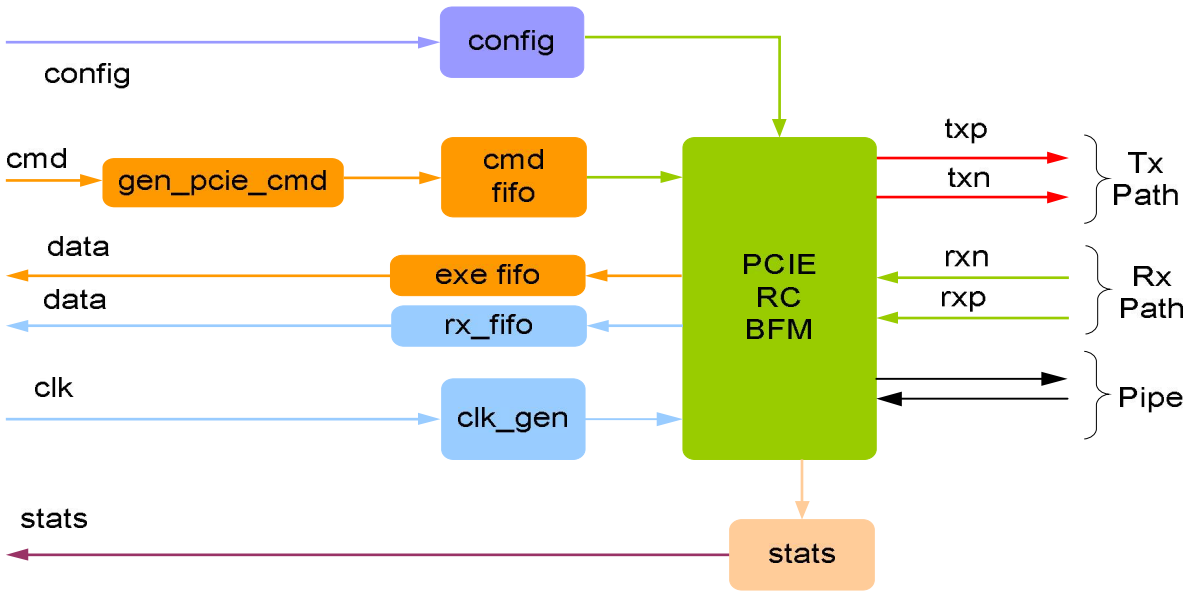
PCIE Verification IP Topology



PCIE Root Complex Behavior

PCIE Root Complex BFM acts as a transmitter, receiver. PCI Express Root BFM is first configured with different configuration parameters. Configuration parameters are scrambler enable, speed of operation, transmit FIFO depth, receive FIFO depth, number of lanes. Error insertion can be performed for common serial data transmission errors, scrambler, link layer errors, Transport layer errors. FIFO's are used to store data received and transmitted during serial.

BFM supports rich set of command generation to generate all PCIE commands.

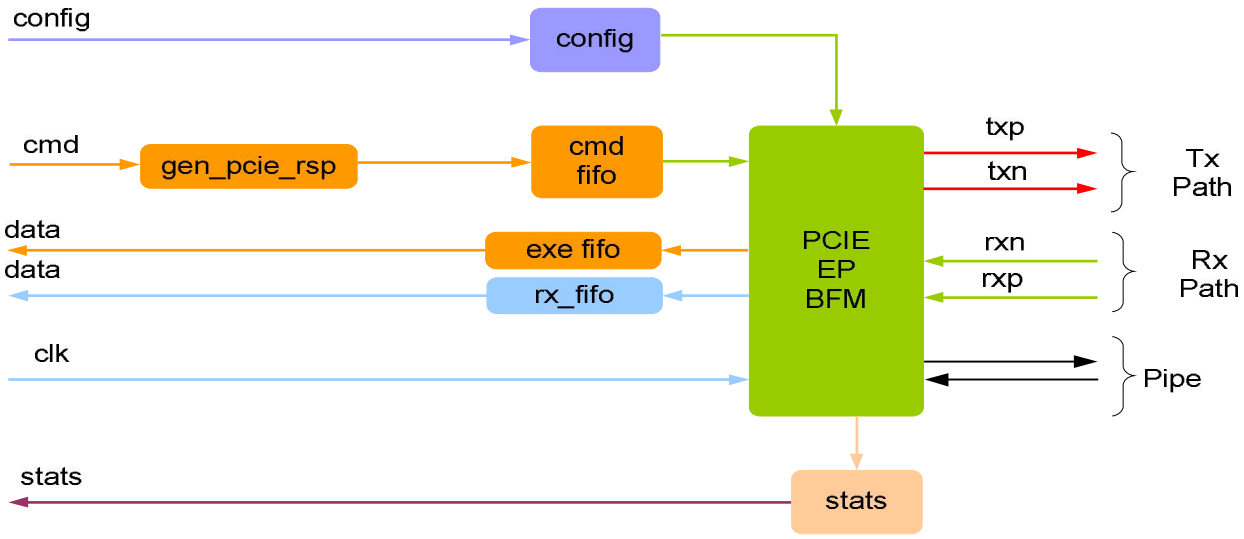


At each stage of transmission and receptions, callbacks are executed for giving control to user to processing the data being transmitted and received. User can change the default behavior to inject errors or create corner cases for testing. Status counters are updated at the end of transmission and reception.

PCI End Point Behavior

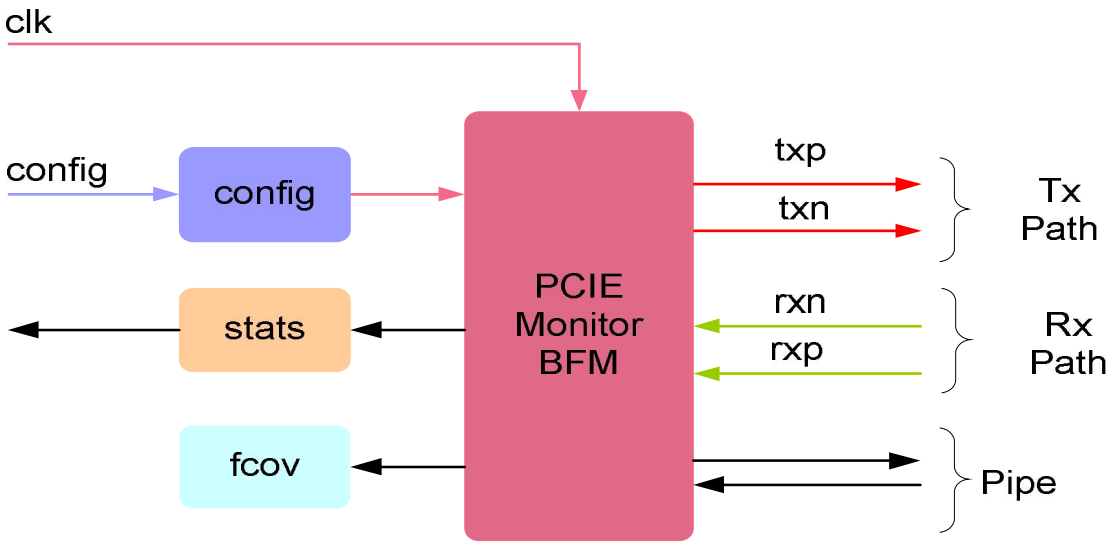
PCIE end point BFM acts as a transmitter, receiver. PCI End point BFM is first configured with different configuration parameters. Configuration parameters are scrambler enable, speed of operation, transmit FIFO depth, receive FIFO depth, number of lanes etc. Error insertion can be performed for common serial data transmission errors, scrambler, link layer errors, Transport layer errors. FIFO's are used to store data received and transmitted during serial.

For type of command that End Point BFM receives, user can control how to respond. Response can either be controlled using callbacks or by populating response buffers with gen_pcie_rsp command.



At each stage of transmission and receptions, callbacks are executed for giving control to user to processing the data being transmitted and received. User can change the default behavior to inject errors or create corner cases for testing. Status counters are updated at the end of transmission and reception.

Monitor Behavior



Monitor is first configured with different configuration parameters. A monitor monitors the both txp/txn and rxn/rxp (transmit and receive path) of PCIE bus for protocol. Monitor also keeps track of all the access on bus, and these stats can be accessed any time during simulation. Protocol checking begins after a valid reset, or without a reset if configured for this condition.

The Monitor also logs all transactions into a file that can be configured through the use of log methods. The Monitor has the same configuration parameters as the PCIE End Point BFM.
PCIE Monitor BFM connects to functional coverage for both transmit and receive path. Functional coverage is written to allow greater reuse of functional coverage points.

Supported Simulators

- VCS
- NC-SIM
- Modelsim
- Questasim

Smart DV Technologies India Private Limited
14/B, 2nd Cross, SR Layout,
Bangalore, India : 560017
E-Mail : info@smart-dv.com
http://www.smart-dv.com