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PMBus Verification IP

Datasheet March 2012 – Version 2.0

Overview

The process of verification is getting complex with every passing year; this is due to the fact that complexity of chips are increasing. With such an increasing design complexity, verification tends to consume up to 60-80% project resources and often represents a bottleneck. Having all this in mind, SmartDV has developed number of Verification IP's, which has been created by verification engineers with decades of experience in verifying complex chips.

The SmartDV Verification IP (VIP) for PMbus provides an efficient and simple way to verify the PMBus bidirectional two-wire bus. The SmartDV VIP for PMBus is fully compliant with version 1.2 of the PMBus Bus Specification and provides the following features:

- Supports Complete PMbus Command set.
- Operates as a Master, Slave, or both. The role of the model can change dynamically according to the
  stimulus applied to the model, no configuration parameters are needed to switch between them. As a Master, the model can Start/Stop all possible transfers. In addition, as a Slave device it can detect Start/Stop conditions and perform data transfers according to the initiator request.

Features

- mplemented in **Unencrypted OpenVera, Verilog, SystemC and SystemVerilog**.
- Supported RVM, AVM, **VMM**, **OVM, UVM** and non-standard verify env.
- Full PMBus Master and Slave functionality.
- Supports all the PMBus commands as per the specs.
- Supports all the extended and normal command codes
- Supports programmable clock frequency of operation.
- Support ARP command generation and response.
- Support Timeout detection and generation.
- Bus-accurate timing.
- PEC support
- Supports master/slave arbitration and clock synchronization.
- Glitch insertion and detection.
- Callbacks in master, slave and monitor for user processing of data
- Supports insertion of errors
  - Master abort in middle of transaction.
  - ACK on last read phase.
  - Master continue on NACK after write NACK from salve.

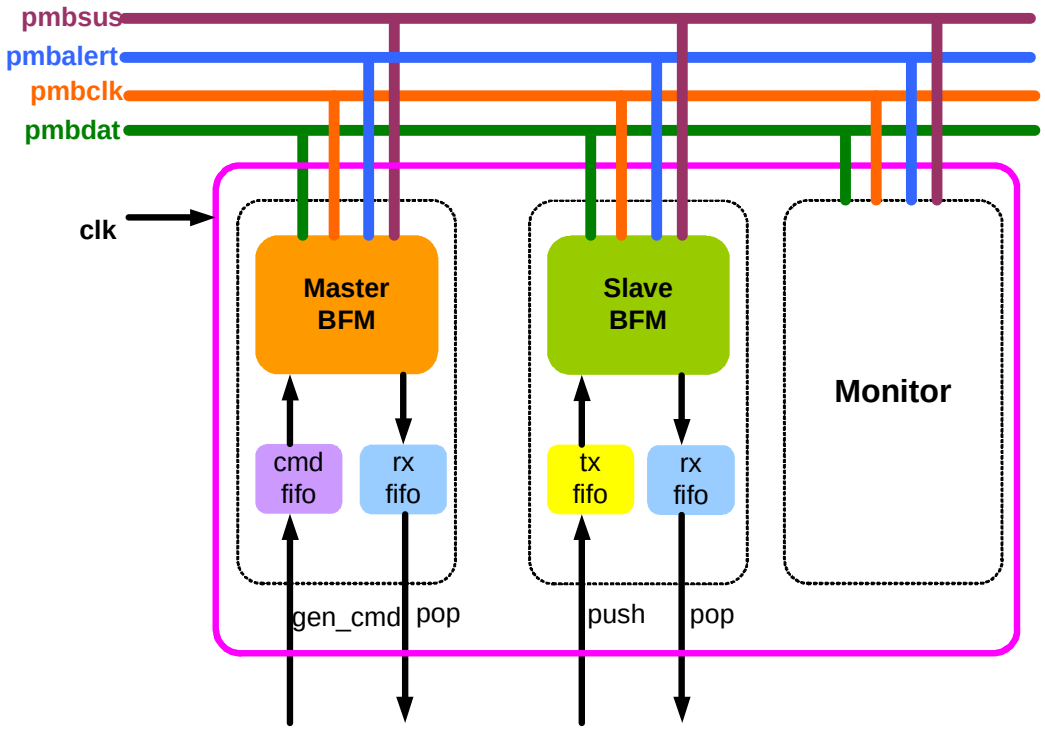
- Random and Periodic clock period stretching by slave.
- Random Write NACK insertion by slave.
- PEC Error.
- Glitch insertion.
- Timeout error insertion.

- Notifies the testbench of significant events such as transactions, warnings, timing and protocol violations.
- PMBus Verification IP comes with **complete testsuite** to test every feature of PMBus specification.

Benefits

- Faster testbench development and more complete verification of PMBus designs.
- Simplifies results analysis.
- Integrates easily into **OpenVera, SytemVerilog, Verilog, Specman, SystemC**
- Runs in every major simulation environment

PMBus Verification IP Topology



Master Behavior

Each master is first configured with different configuration parameters. The master then initiates requests based on various PMBus Commands and general call transfers from the testbench. Read data from slave is placed in RX Byte Fifo. The master also arbitrates the bus using the serial data (PMBDAT) and PMBCLK lines and can be configured to react in different ways if the bus is not free. Arbitration follows the rules set by the PMBus protocol. Forcing the

Master to abort the transfer at the specified bit position supports error injection.

Slave Behavior

Each slave is first configured with different configuration parameters. A slave device monitors the bus to determine if it has been selected for a transfer request. It will always respond to a transfer request if it has been selected. The slave responds to read requests by sending data which can be fed through its TX Byte Fifo. For write requests, the slave receives data transmitted by the master and passes it to the RX fifo. The slave can be made to act erroneously by forcing it to respond with an acknowledgment (or no acknowledgment) to transfer requests. Slave BFM supports user callbacks for read and write command processing. Thus it is possible to build any kind of application using callbacks.

Monitor Behavior

Monitor is first configured with different configuration parameters. A monitor monitors the PMBus bus for protocol errors and timing errors. Monitor also keeps track of all the access on bus, and these stats can be accessed any time during simulation.

Supported Simulators

- VCS
- NC-Sim
- ModelSim
- Questasim

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