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RapidIO Verification IP

September 2010 – Version 3.0

Overview

The process of verification is getting complex with every passing year; this is due to the fact that complexity of chips is increasing. With such an increasing design complexity, verification tends to consume up to 60-80% project resources and often represents a bottleneck. Having all this in mind, SmartDV has developed number of Verification IP's, which has been created by verification engineers with decades of experience in verifying complex chips.

The SmartDV Verification IP (VIP) for RapidIO provides an efficient and simple way to verify and monitor the RapidIO and collect data on bus. The SmartDV VIP for RapidIO Verification IP is fully compliant with RapidIO Specification 1.3, 2.0 and 2.1

- Supports all types of RapidIO Packet types.
- Operates as INITIATOR, TARGET, INITIATOR/TARGET, MONITOR

Features

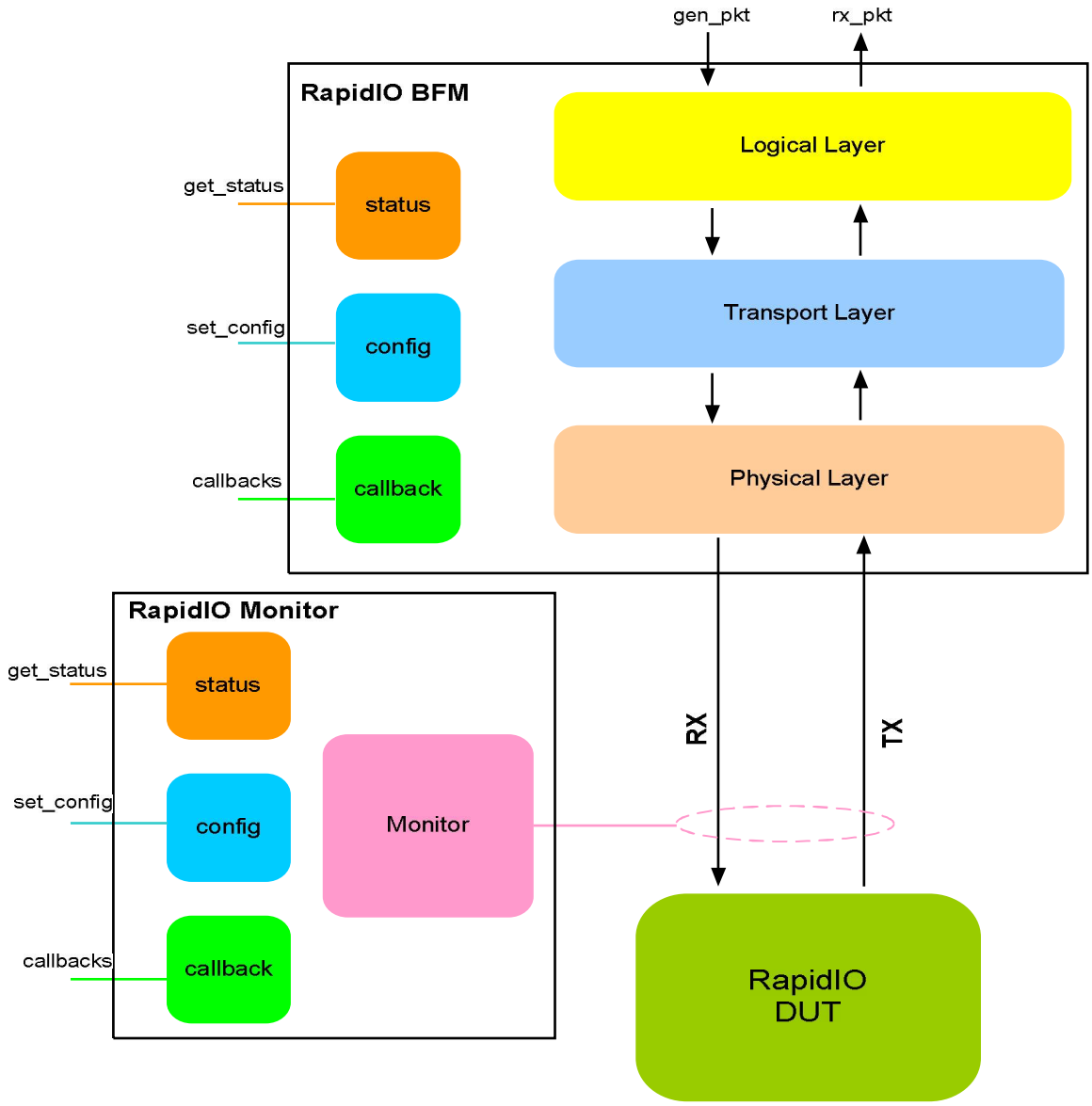
- Implemented natively in OpenVera, Verilog, SystemC, Specman E and SystemVerilog
- Supported RVM, AVM, VMM, OVM, UVM and non-standard verify env.
- Supports RapidIO specification 1.3,2.0 and 2.1.
- Supports Serial 1x/2x/4x/8x and 16x Physical lanes.
- Supports XTBI like interface for testing after PCS layer.
- Supports XGMII like interface for testing before PCS layer.
- Supports 6.25Gbaud/s, 5Gbaud/s,3.125 Gbaud/s, 2.5 Gbaud/s, 1.25 Gbaud/s.
- 66, 50, or 34-bit addressing on the RapidIO interface.
- Supports Parallel Physical 8/16 bits interfaces.
- Supports all types of packets and sizes.
- Supports 8-bit or 16-bit device IDs
- Automatic freeing of resources used by acknowledged packets
- Supports I/O system, message passing and globally shared distributed memory (GSM).
- Supports communication with mailboxes via messages.
- Supports generation and reaction to flow control.
- Supports out of order transaction delivery based on the prioritization.
- Supports critical request flow ordering.
- Very flexible to insert errors in serial lanes.
- Supports Error Management Extensions.

- Provides error injection and error detection with a wide variety of error types. Which includes,
    1. Under and oversize packet.
    2. CRC errors
    3. Invalid code group insertion
    4. Invalid /K/ characters insertion
    5. Lane Skew insertion
    6. Received S bit parity error on packet/control symbol
    7. Error on control symbol
    8. Oversized and undersized packets
    9. unsupported packet types
- Supports cancellation and retrying of packets mechanisms.
- Support all types of timing and protocol violation detection.
- Supports constraints Randomization.
- Status counters to keep track of various events.Which includes
    1. Corrupted/uncorrupted packets
    2. uncorrupted/uncorrupted control symbols
    3. Type of packet
    4. CRC error
    5. Total number of errors detected
- Supports callbacks for user to get packets or errors in INITIATOR/TARGET and monitor.
- Rapidio verification IP comes with complete testsuite to test every feature of Rapidio spec and also as per RIO LAB testsuite.
- Functional coverage for each functional condition in env.
- Notifies the testbench of significant events such as transactions, warnings, timing and protocols violations.

Benefits

- Faster test bench development and more complete verification of RAPIDIO designs.
- Simplifies results analysis.
- Integrates easily into **OpenVera, SytemVerilog, SystemC, Verilog**.
- Runs in every major simulation environment.

RapidIO Verification IP Topology



RapidIO BFM Behavior

RapidIO BFM is first configured with different configuration parameters; SmartDV's RapidIO verification supports rich set of configuration parameters to control each and every possible configuration parameter. This is stored in config object in above block diagram. User is provided with rich set of methods to generate different types of packets on the RapidIO physical interface. User has access to advance error insertion methods, which allow user to insert errors in any layer, like inserting CRC error logical layer or inserting disparity error in PCS.

RapidIO receiver receives various packets based on the user response programming, it

responds in out of order, responds after certain delay, errors responses and retry response. RapidIO receiver has the capability to detect various error like invalid field values, disparity errors, invalid /K/ characters. Receiver supports user controlled flow control packet generator or buffer depth based flow control generation.

During execution of above methods, callbacks are executed, where user can override the default behavior of the RapidIO BFM. At the end of execution of methods, status counters are updated. User can access this counters anytime during simulation.

User can create complex sequence of commands with help of generic command methods (Not shown in block diagram). RapidIO BFM can also be configured to log all the access into a log file, with different debug levels. This can be later used for post processing.

RapidIO Monitor Behavior

Monitor is first configured with different configuration parameters. This is stored in config object in above block diagram. After a valid reset, whenever a valid access is detected, monitor collects complete packet and data associated with command and executes the callback. Also status counters are updated to reflect the current status of the access.

A monitor monitors the RapidIO bus for protocol errors and timing errors. Monitor also keeps track of all the access on bus, and these stats can be accessed any time during simulation. RapidIO monitor can also be configured to log all the access into a log file, with different debug levels. This can be later used for post processing. Monitor implements functional coverage.

Supported Simulators

- VCS
- NC-Sim
- ModelSim
- Questasim

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