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SATA Verification IP

Datasheet April 2012 – Version 1.0

Overview

The process of verification is getting complex with every passing year; this is due to the fact that complexity of chips are increasing. With such an increasing design complexity, verification tends to consume up to 60-80% project resources and often represents a bottleneck. Having all this in mind, SmartDV has developed number of Verification IP's, which has been created by verification engineers with decades of experience in verifying complex chips.

The SmartDV Verification IP (VIP) for SATA provides an efficient and simple way to verify the SATA 1.0/2.0/3.0 protocol bus. The SmartDV VIP for SATA is fully compliant with Serial ATA Revision 3.0 Specification and provides the following features:

- Supports full SATA specification.
- Operates as SATA Host, SATA Device and SATA Monitor.

Features

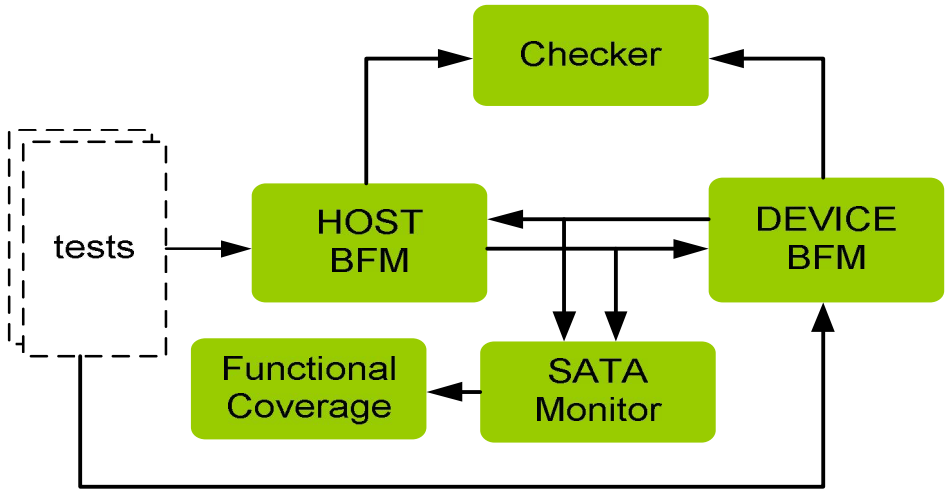
- Implemented in **Unencrypted OpenVera, Verilog, SystemC and SystemVerilog**.
- Supported RVM, AVM, **VMM**, **OVM**, **UVM** and non-standard verify env.
- Supports 1.5, 3 and 6 Gbps speeds
- Supports serial (1 bit) and parallel (10/20/40 bit) interface
- 8b/10b encoding and decoding, Error injection.
- Configurable OOB signals and speed of operation
- Configurable phy layer timers
- Optional DC-IDLE pin
- User defined primitive transmission
- Single or multi-bit error injection
- Complete link layer state machines
- Disparity error injection and checking
- User defined primitives & frame transmission
- Supports link layer power modes
- SYNC injection during FIS transfer
- Randomized/directed CRC error injection and checking
- Ability to enable/disable scrambling on the fly
- Programmable enable/disable & duration of DMAT, CONT and HOLD primitives
- Callback functions for state transitions, primitive and FIS reception/transmissioon OOB transmission/reception and speed change

- Supports LBA with HDD size configuration
- APIs providing backdoor access to HDD
- Programmable auto-activate support using configuration
- Supports all standard ATA command sets including NCQ
- Configurable FIS latencies, FIFO depths and FIS size
- Supports asynchronous notification
- Callbacks in Host, Device and monitor for user processing of data
- Notifies the testbench of significant events such as transactions, warnings, timing and protocol violations.
- SATA Verification IP comes with **complete testsuite** to test every feature of SATA specification**.**
- Functional coverage for complete SATA features.

Benefits

- Faster testbench development and more complete verification of SATA designs.
- Simplifies results analysis.
- Integrates easily into **OpenVera, SytemVerilog,SystemC,Verilog**
- Runs in every major simulation environment

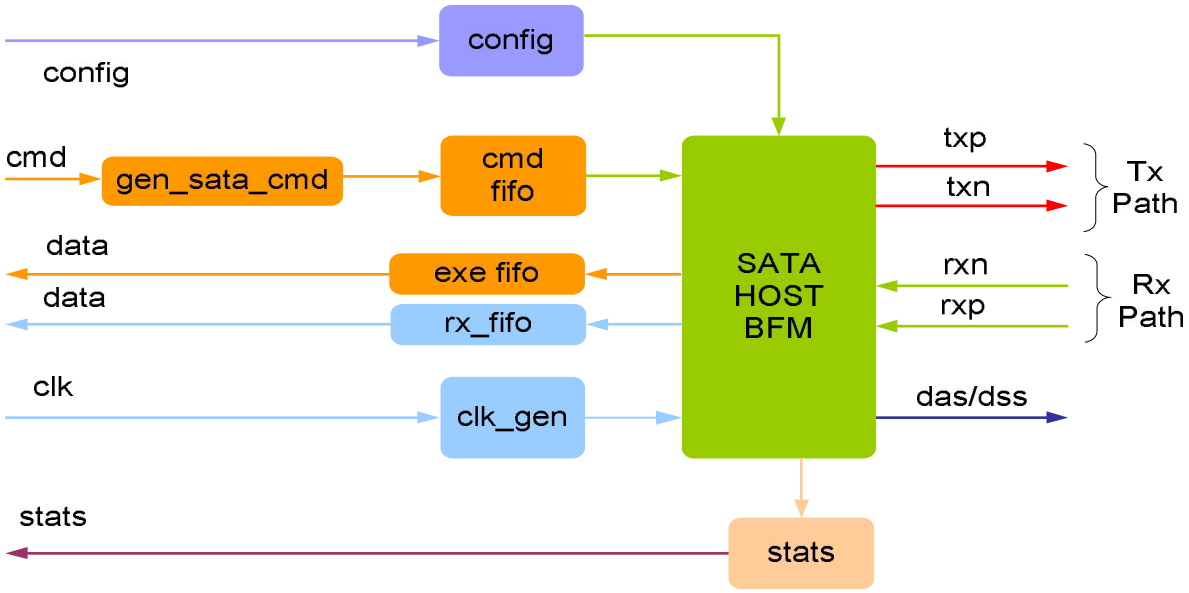
SATA Verification IP Topology



SATA HOST Behavior

SATA Host BFM acts as a transmitter, receiver. SATA Host BFM is first configured with different configuration parameters. Configuration parameters are scrambler enable, speed of operation, transmit FIFO depth, receive FIFO depth. Error insertion can be performed for common serial data transmission errors, scrambler, link layer errors, Transport layer errors. FIFO's are used to store data received and transmitted during serial.

SATA host BFM supports rich set of command generation to generate all SATA commands.

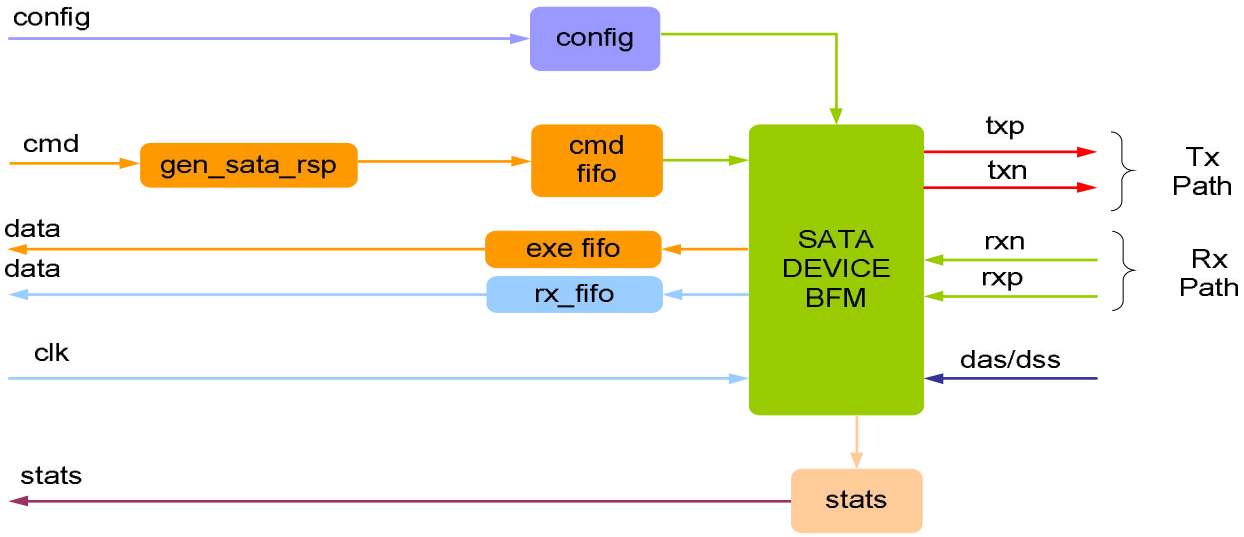


At each stage of transmission and receptions, callbacks are executed for giving control to user to processing the data being transmitted and received. User can change the default behavior to inject errors or create corner cases for testing. Status counters are updated at the end of transmission and reception.

SATA Device Behavior

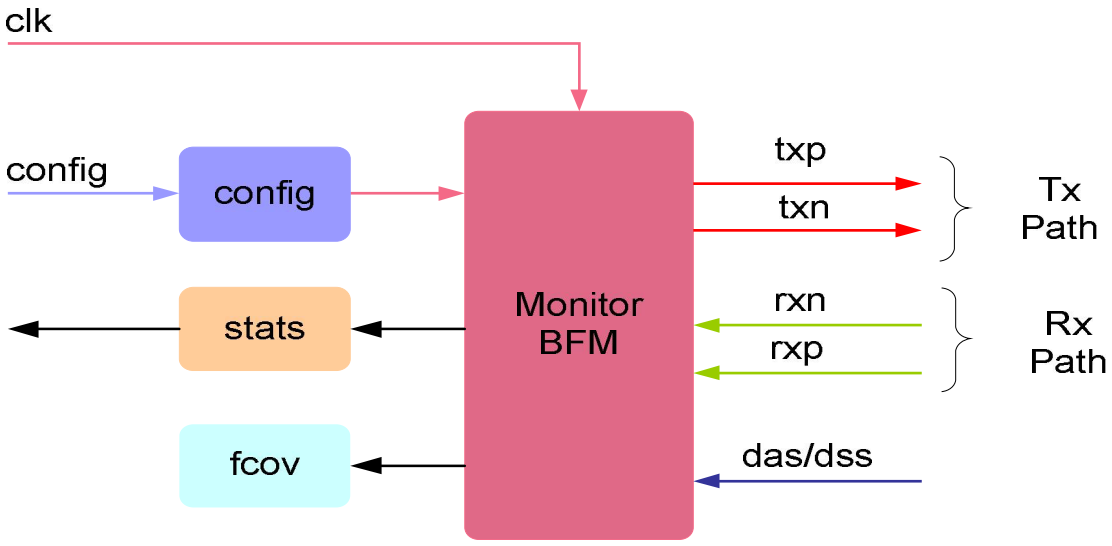
SATA device BFM acts as a transmitter, receiver. SATA device BFM is first configured with different configuration parameters. Configuration parameters are scrambler enable, speed of operation, transmit FIFO depth, receive FIFO depth. Error insertion can be performed for common serial data transmission errors, scrambler, link layer errors, Transport layer errors. FIFO's are used to store data received and transmitted during serial.

For type of command that Device BFM receives, user can control how to respond. Response can either be controlled using callbacks or by populating response buffers with gen_sata_rsp command.



At each stage of transmission and receptions, callbacks are executed for giving control to user to processing the data being transmitted and received. User can change the default behavior to inject errors or create corner cases for testing. Status counters are updated at the end of transmission and reception.

Monitor Behavior



Monitor is first configured with different configuration parameters. A monitor monitors the both txp/txn and rxn/rxp (transmit and receive path) of SATA bus for protocol. Monitor also keeps track of all the access on bus, and these stats can be accessed any time during simulation. Protocol checking begins after a valid reset, or without a reset if configured for this condition. The Monitor also logs all transactions into a file that can be configured through the use of log methods. The Monitor has the same configuration parameters as the SATA Device BFM.

SATA Monitor BFM connects to functional coverage for both transmit and receive path. Functional coverage is written to allow greater reuse of functional coverage points.

Supported Simulators

- VCS
- NC-SIM
- Modelsim
- Questasim

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