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SDIO Verification IP

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Overview

The process of verification is getting complex with every passing year; this is due to the fact that complexities of chips are increasing. With such an increasing design complexity, verification tends to consume up to 60-80% project resources and often represents a bottleneck. Having all this in mind, SmartDV has developed number of Verification IP's, which have been created by verification engineers with decades of experience in verifying complex chips.

SDIO 1.0, 2.0 and 3.0 VIP is an advanced solution in the market for the verification of SDIO 1.0/2.0/3.0 implementations. It is adherent with SDIO 1.0/2.0/3.0 standard and supports SPI, SD1, SD4 and SD8. It can generate all command types. The SDIO VIP monitor acts as powerful protocol-checker, fully compliant with SDIO 1.0/2.0/3.0 specifications.

The SmartDV Verification IP (VIP) for SDIO provides an efficient and simple way to verify the SDIO protocol bus. SDIO 1.0/2.0/3.0 VIP includes an extensive test suite covering all the possible scenarios and SDIO conformance norms. SDIO 1.0/2.0/3.0VIP can perform all protocol tests as test bench and moreover it allows an easy generation of a very high number of patterns and a set of specified patterns to stress the DUT.

- Operates as SDIO HOST, SLAVE and SDIO monitor.
- Supports MMC and eMMC protocols.

Features

- Implemented in **Unencrypted OpenVera, SystemVerilog, Verilog, SystemC and Specman E.**
- Supported RVM, AVM, VMM, OVM, UVM and non-standard verify env.
- SDIO Specification 1.0/2.0/3.0 compliant.
- Supports SDIO, SD Memory, SD Combo card and Multi-media cards
- Easily configurable to work as SDIO aware or non-SDIO aware Host controller
- Card detection on DAT [3] line in SD mode and CS line in SPI mode
- Re-initialization of combo card in either SDIO only mode or SD memory only mode
- Command level features such as resetting the card, setting bus width and changing bus mode (SD to SPI)
- 1-bit, 4-bit, 8-bit SD bus mode and SPI bus mode
- All version 3.0 features supported such as speed class, tuning, and voltage and block size control.
- Supports all features of SD specification Part 1 eSD(Embedded SD) addendum

- Supports all features of SDIO card Type-A specification for Bluetooth version 1.00
- Supports all features of SDIO card Type-B specification for Bluetooth version 1.00
- All UHS1 modes – SDR50/SDR104/DDR50 supported.
- Supports read-write, read-only cards
- Switch function command supports Bus speed mode, command system, drive strength and future function
- Set block count(CMD23) command is supported
- Supports different memory capacities given below:
  - Standard Capacity SD Memory Card (SDSC): Up to and including 2 GB
  - High Capacity SD Memory Card (SDHC): More than 2GB and up to and including 32GB
  - Extended Capacity SD Memory Card (SDXC): More than 32GB and up to and including 2TB
- Supports e-MMC standard and high capacity standards JESD840A42, JESD84-A441, and JESD84-B45, supports MMC standard JESD840B42.
- Low speed mode, full speed mode and high speed mode operations
- Single byte, single block, multiple block (finite and infinite) transfers and MMC stream transfer operations
- Direct command during data transfer (SD mode only)
- Read wait operation and allows read wait control by stopping clock and by asserting DAT [2] line low
- Asynchronous and synchronous abort mechanism
- Suspend/Resume card operation
- Lock-unlock and erase operation card features
- SD 1-bit , SPI mode interrupt and SD 4-bit mode card interrupts
- Clock disable and interrupt wake up card features
- Bus-accurate timing
- Detects and reports the following errors.
  - Out of range error
  - Address misalign error
  - CRC error
  - Switch error
  - Illegal command error
  - Block length error
  - Lock-unlock failed error
  - Erase sequence error
  - Direction bit error
  - Stuff bit error
  - Erase param error
  - Parameter error
  - Invalid voltage error
  - Reserved bit error
  - Function number error
  - WP violation error
  - CSD/CID over write error
- Protocol Checker fully compliant with SDIO Specification 1.0/2.0/3.0 compliant.
- SDIO Verification IP comes with **complete testsuite** to test every feature of SDIO

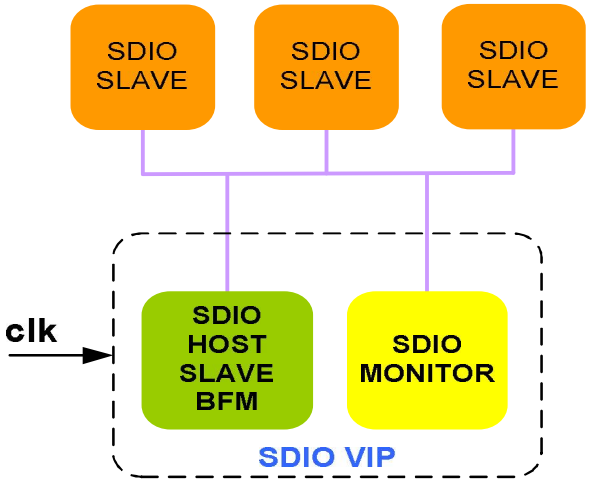
specification.

- Monitors, detects and notifies the test bench of significant events such as transactions, warnings, timing and protocol violations
- Status counters for various events on bus.
- Functional coverage for complete SDIO features

Benefits

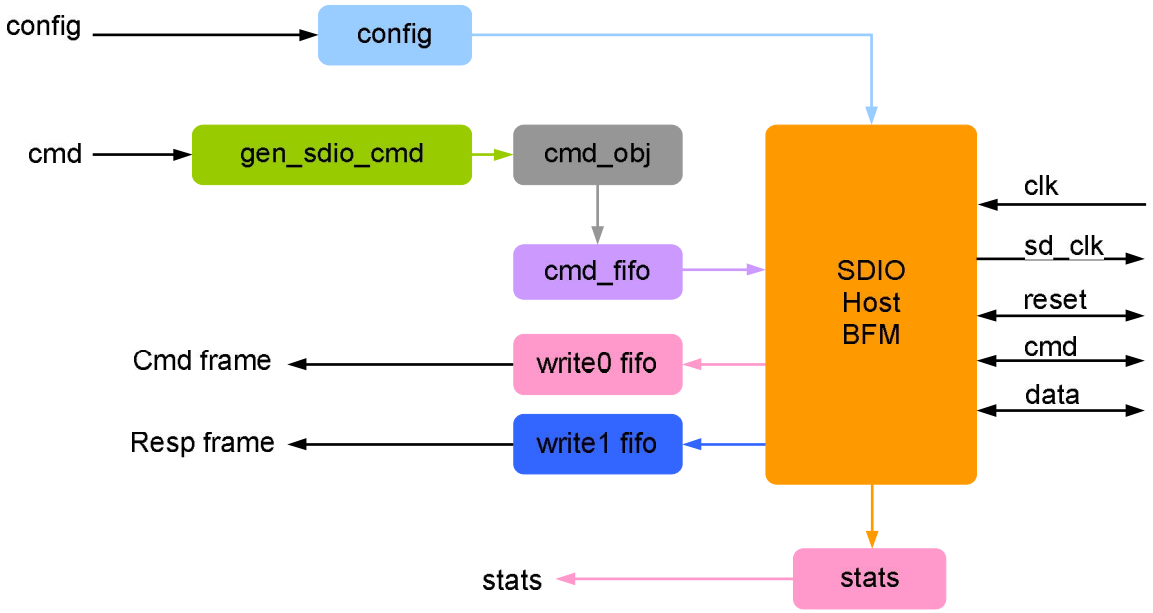
- Faster testbench development and more complete verification of SDIO designs.
- Simplifies results analysis.
- Easy to use command interface simplifies testbench control and configuration of Host and slave.
- Runs in every major simulation environment.

SDIO Verification IP Topology



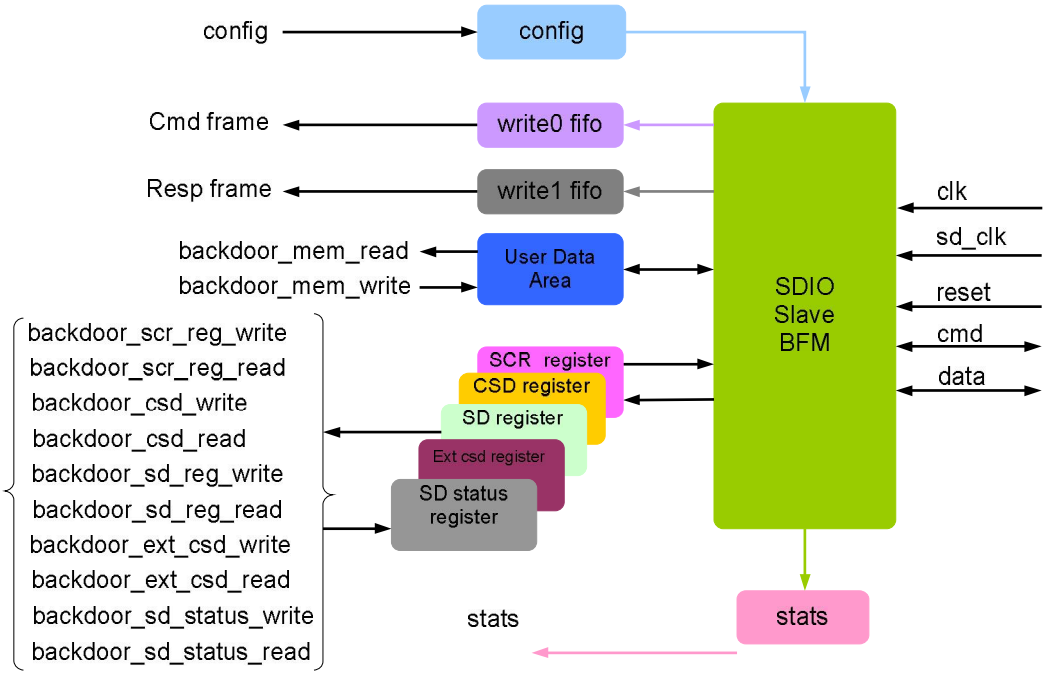
Host Behavior

SDIO Host BFM is first configured with various configuration parameters like SKIP Init sequence, data width, SD bus mode, write data delay, command to command delay, and FIFO depth. User has access to rich set of SDIO commands to generate various types of accesses on the SDIO bus; these commands are flexible to allow full randomization of various fields of the command. For commands that get response from the slave, they are placed in HOST response FIFO. Status counters are updated at the end of transmission of command. Error injection is supported by forcing the host to abort the transfer at the specified position



Slave Behavior

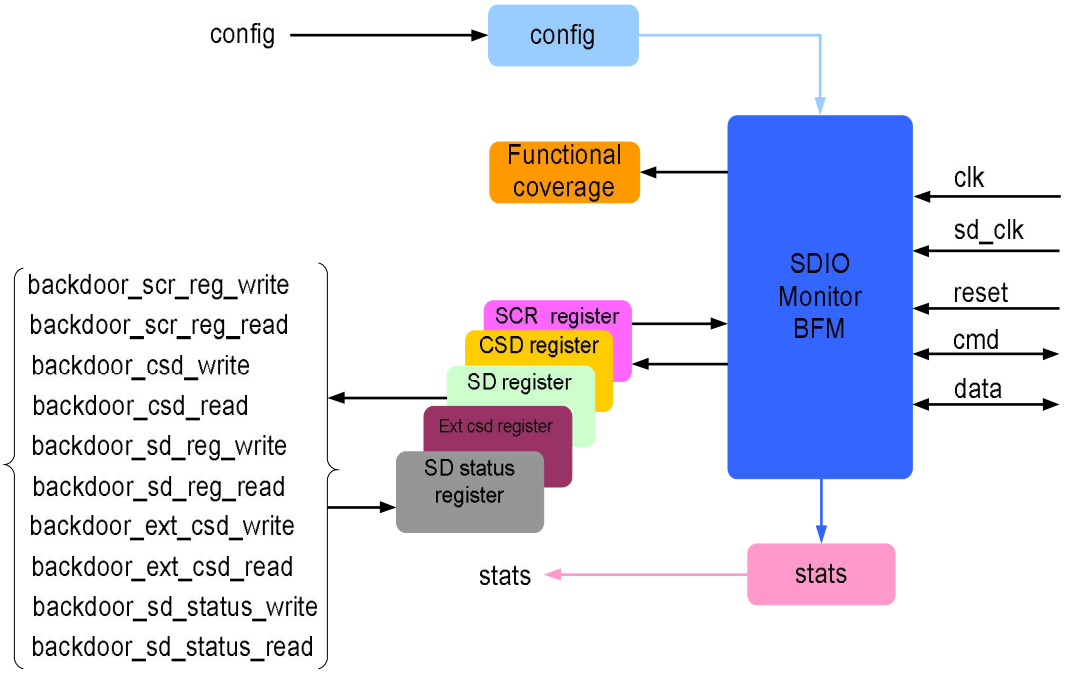
SDIO Slave is first configured with different configuration parameters. The slave keeps monitoring the bus for a valid command from the host. Depending on command type slave responds to the HOST.



For a write command, slave receives data from host and writes to internal memory model. For the read command, slave sends the data to host from the memory model or FIFO. Slave BFM behaves as per the device configured. At the end of command reception, status counters are updated.

Monitor Behavior

Monitor is first configured with different configuration. Monitor monitors the SDIO bus for protocol errors and timing errors. Monitor also keeps track of all the accesses on the bus and updates the status counters. These status counters can be accessed any time during simulation. The monitor also implements functional coverage points which user can use to measure the quality of verification.



Supported Simulators

- VCS
- NC-Sim
- Modelsim
- Questasim

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