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eMMC Verification IP

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Overview

The process of verification is getting complex with every passing year; this is due to the fact that complexities of chips are increasing. With such an increasing design complexity, verification tends to consume up to 60-80% project resources and often represents a bottleneck. Having all this in mind, SmartDV has developed number of Verification IP's, which have been created by verification engineers with decades of experience in verifying complex chips.

eMMC VIP is an advanced solution in the market for the verification of eMMC JESD84-A441 and JESD84-B45 implementations. It is adherent with eMMC JESD84-A441 and JESD84-B45 standard and supports SD1, SD4 and SD8. It can generate all command types. The eMMC VIP monitor acts as powerful protocol-checker, fully compliant with eMMC JESD84-A441 and JESD84-B45 specifications.

The SmartDV Verification IP (VIP) for eMMC provides an efficient and simple way to verify the EMMC protocol bus. eMMC VIP includes an extensive test suite covering all the possible scenarios and eMMC conformance norms. eMMC VIP can perform all protocol tests as test bench and moreover it allows an easy generation of a very high number of patterns and a set of specified patterns to stress the DUT.

- Operates as eMMC HOST, SLAVE and eMMC monitor.

Features

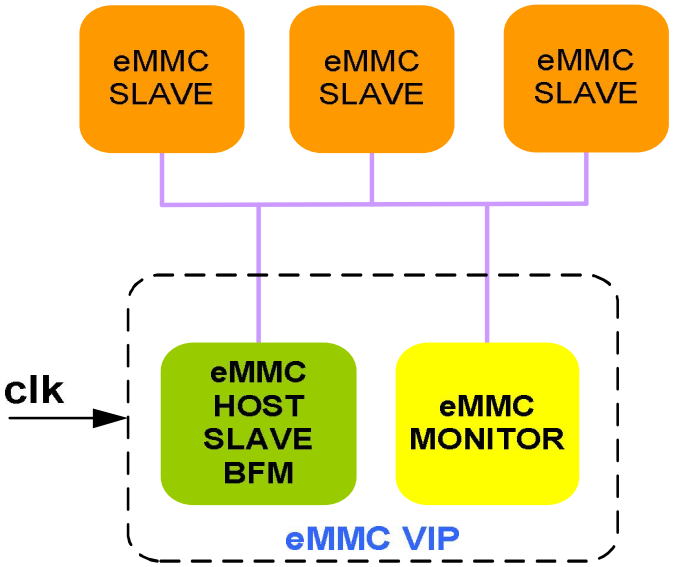
- Implemented in **Unencrypted OpenVera, SystemVerilog, Verilog, SystemC and Specman E.**
- Supported RVM, AVM, VMM, OVM, UVM and non-standard verify env.
- Supports eMMC standard JESD84-A441 and JESD84-B45
- Supports different data bus width modes : 1-bit, 4-bit, 8-bit
- Supports higher than 2GB densities of memory
- Supports hardware reset signal
- Supports high speed boot operation
- Single byte, single block, multiple block (finite and infinite) transfers and MMC stream transfer operations
- Supports stream write/read

- Supports send tuning block(CMD21) command
- Supports HS200 mode
- Supports data protection mechanism like password, permanent ,power-on and temporary
- Supports data removable mechanism
- Supports high voltage & dual voltage
- Supports single data rate & dual data rate
- Supports boot and alternate boot operation
- Bus-accurate timing
- Detects and reports the following errors.
  - Out of range error
  - Address misalign error
  - CRC error
  - Switch error
  - Illegal command error
  - Block length error
  - Lock-unlock failed error
  - Erase sequence error
  - Direction bit error
  - Stuff bit error
  - Erase param error
  - Parameter error
  - Invalid voltage error
  - Reserved bit error
  - WP violation error
  - CSD/CID over write error
- Protocol Checker fully compliant with EMMC Specification JESD84-A441 and JESD84-B45 compliant.
- EMMC Verification IP comes with **complete testsuite** to test every feature of EMMC specification.
- Monitors, detects and notifies the test bench of significant events such as transactions, warnings, timing and protocol violations
- Status counters for various events on bus.
- Functional coverage for complete eMMC features

Benefits

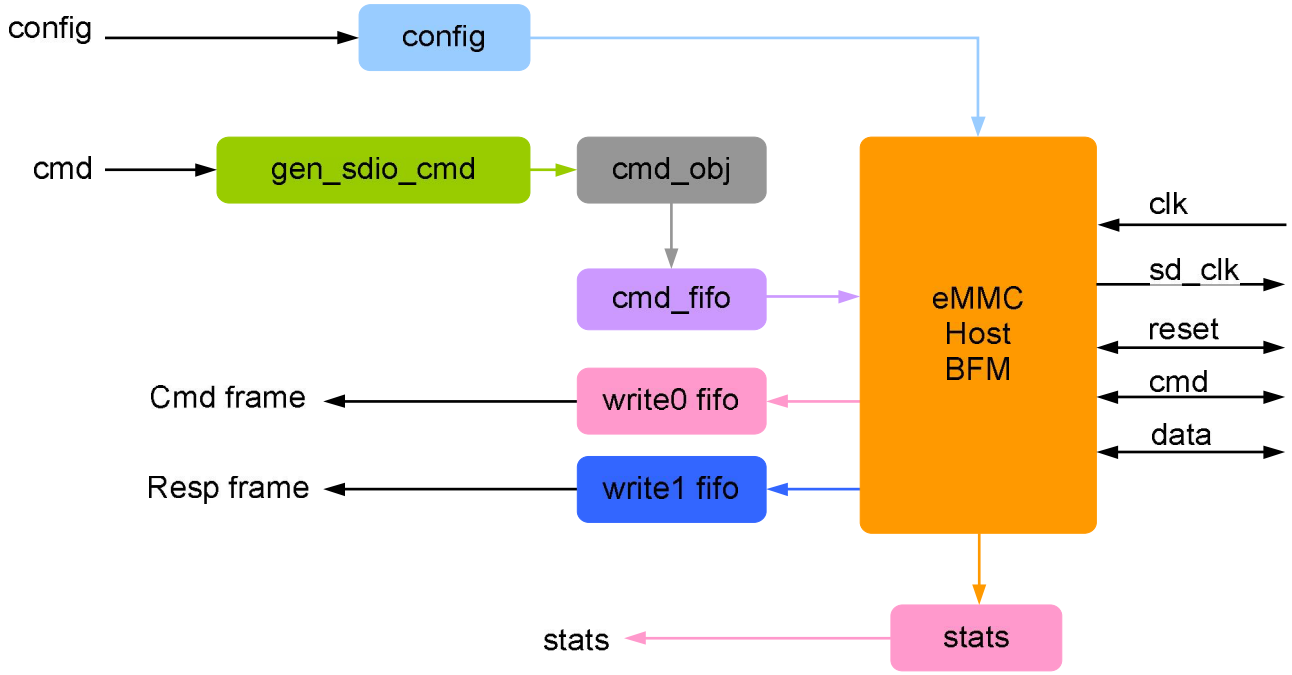
- Faster testbench development and more complete verification of EMMC designs.
- Simplifies results analysis.
- Easy to use command interface simplifies testbench control and configuration of Host and slave.
- Runs in every major simulation environment.

eMMC Verification IP Topology



Host Behavior

eMMC Host BFM is first configured with various configuration parameters like write data delay, command to command delay, and FIFO depth.

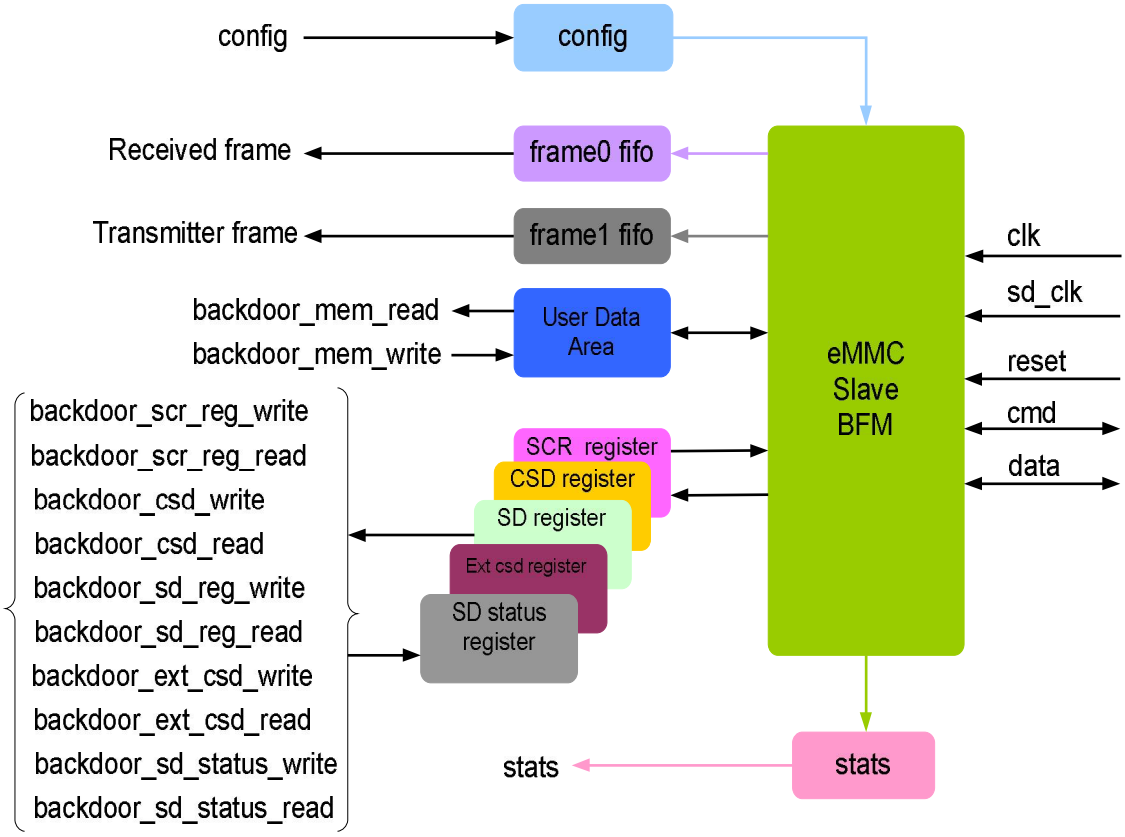


User has access to rich set of eMMC commands to generate various types of accesses

on the eMMC bus; these commands are flexible to allow full randomization of various fields of the command. For commands that get response from the slave, they are placed in HOST response FIFO. Status counters are updated at the end of transmission of command. Error injection is supported by forcing the host to abort the transfer at the specified position.

Slave Behavior

eMMC Slave is first configured with different configuration parameters. The slave keeps monitoring the bus for a valid command from the host. Depending on command type slave responds to the HOST.

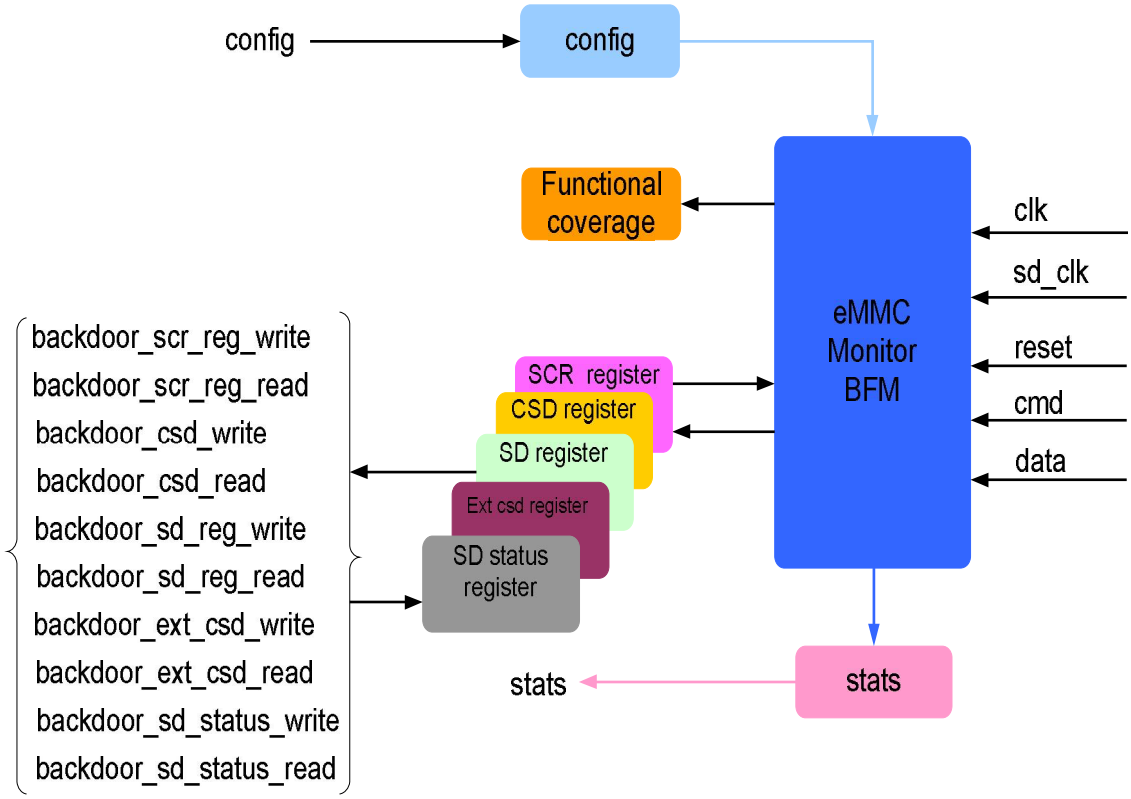


For a write command, slave receives data from host and writes to internal memory model. For the read command, slave sends the data to host from the memory model or FIFO. Slave BFM behaves as per the device configured. At the end of command reception, status counters are updated.

Monitor Behavior

Monitor is first configured with different configuration. Monitor monitors the eMMC bus for protocol errors and timing errors. Monitor also keeps track of all the accesses on the bus and updates the status counters. These status counters can be accessed any time

during simulation. The monitor also implements functional coverage points which user can use to measure the quality of verification.



Supported Simulators

- VCS
- NC-Sim
- Modelsim
- Questasim

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