Smart DV Technologies India Private Limited
14/B, 2nd Cross, SR Layout,
Bangalore, India : 560017
E-Mail : info@smart-dv.com
http://www.smart-dv.com

SDIO UHS-II Verification IP

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Overview

The process of verification is getting complex with every passing year; this is due to the fact that complexities of chips are increasing. With such an increasing design complexity, verification tends to consume up to 60-80% project resources and often represents a bottleneck. Having all this in mind, SmartDV has developed number of Verification IP's, which have been created by verification engineers with decades of experience in verifying complex chips.

SDIO UHS II VIP is an advanced solution in the market for the verification of SDIO UHS-II implementations. It can generate all command types. The SDIO UHS-II VIP monitor acts as powerful protocol-checker, fully compliant with SDIO UHS-II Addendum version1.00 specifications.

The SmartDV Verification IP (VIP) for SDIO UHS-II provides an efficient and simple way to verify the SDIO UHS-II protocol bus. SDIO UHS-II VIP includes an extensive test suite covering all the possible scenarios and SDIO UHS-II conformance norms. SDIO UHS-II VIP can perform all protocol tests as test bench and moreover it allows an easy generation of a very high number of patterns and a set of specified patterns to stress the DUT.

- Operates as SDIO UHS-II HOST, CARD and monitor.

Features

- Implemented in **Unencrypted OpenVera, SystemVerilog, Verilog, SystemC and Specman E.**
- Supported RVM, AVM, VMM, OVM, UVM and non-standard verify env.
- SDIO UHS-II Specification Addendum verszion1.00 compliant.
- Supports bi-directional receiver/transmitter (2ch) supporting both Full Duplex and Half Duplex modes
- Lock-unlock and erase operation card features
- Supports RCLK frequency: 26~56MHz
- Supports fast mode and low power mode
- Supports flow control operations.
- Supports test modes
- Supports power saving modes
- Supports scrambling
- Supports data transaction for SD-TRAN and CM-TRAN
- Supports data transaction transfer length is fixed and infinite for SD-TRAN and

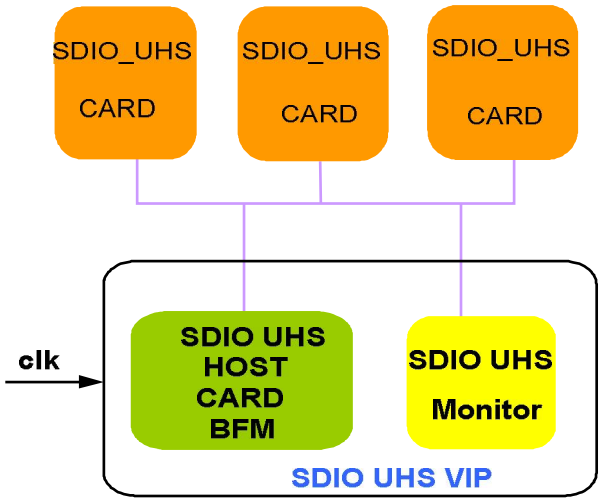
CM_TRAN

- Detects and reports the following errors.
    - Out of range error
    - Address misalign error
    - CRC error
    - Switch error
    - Illegal command error
    - Block length error
    - Lock-unlock failed error
    - Erase sequence error
    - Direction bit error
    - Stuff bit error
    - Parameter error
    - Invalid voltage error
    - Reserved bit error
    - Function number error
    - WP violation error
    - CSD/CID over write error
    - Disparity error insertion
    - Invalid K character error
    - Missing K character error
    - Link layer error injection
    - Initialization error injection
    - Illegal header error
    - Device specific error
    - Retry expiry error
    - Frame error
    - Scrambler error
- Protocol Checker fully compliant with SDIO UHS-II Addendum version1.00 compliant.
- SDIO UHS-II Verification IP comes with **complete testsuite** to test every feature of SDIO UHS-II Addendum version1.00 specification.
- Monitors, detects and notifies the test bench of significant events such as transactions, warnings, timing and protocol violations
- Status counters for various events on bus.
- Functional coverage for complete SDIO UHS-II features

Benefits

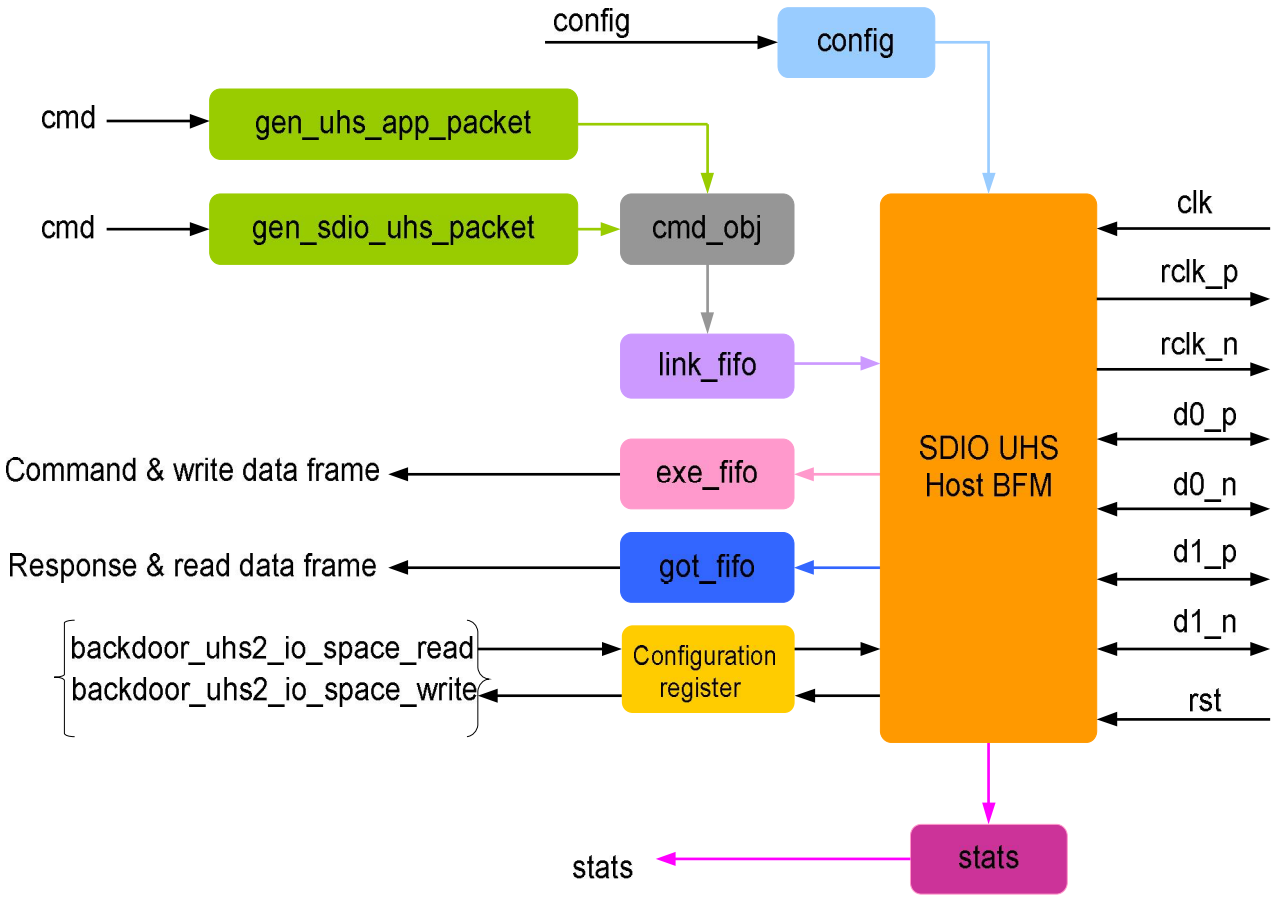
- Faster test bench development and more complete verification of SDIO UHS-II designs.
- Simplifies results analysis.
- Easy to use command interface simplifies test bench control and configuration of Host and slave.
- Runs in every major simulation environment.

SDIO Verification IP Topology

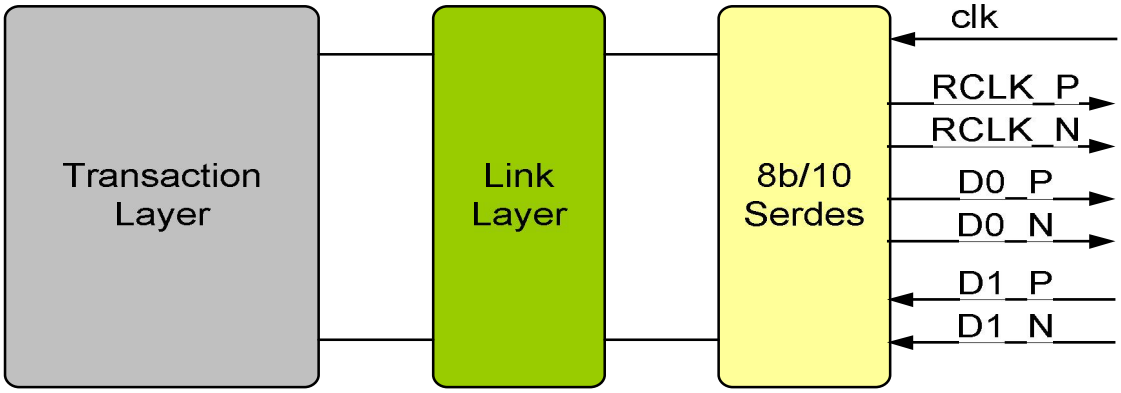


Host Behavior

Note : Legacy interface is not shown In below block diagrams.

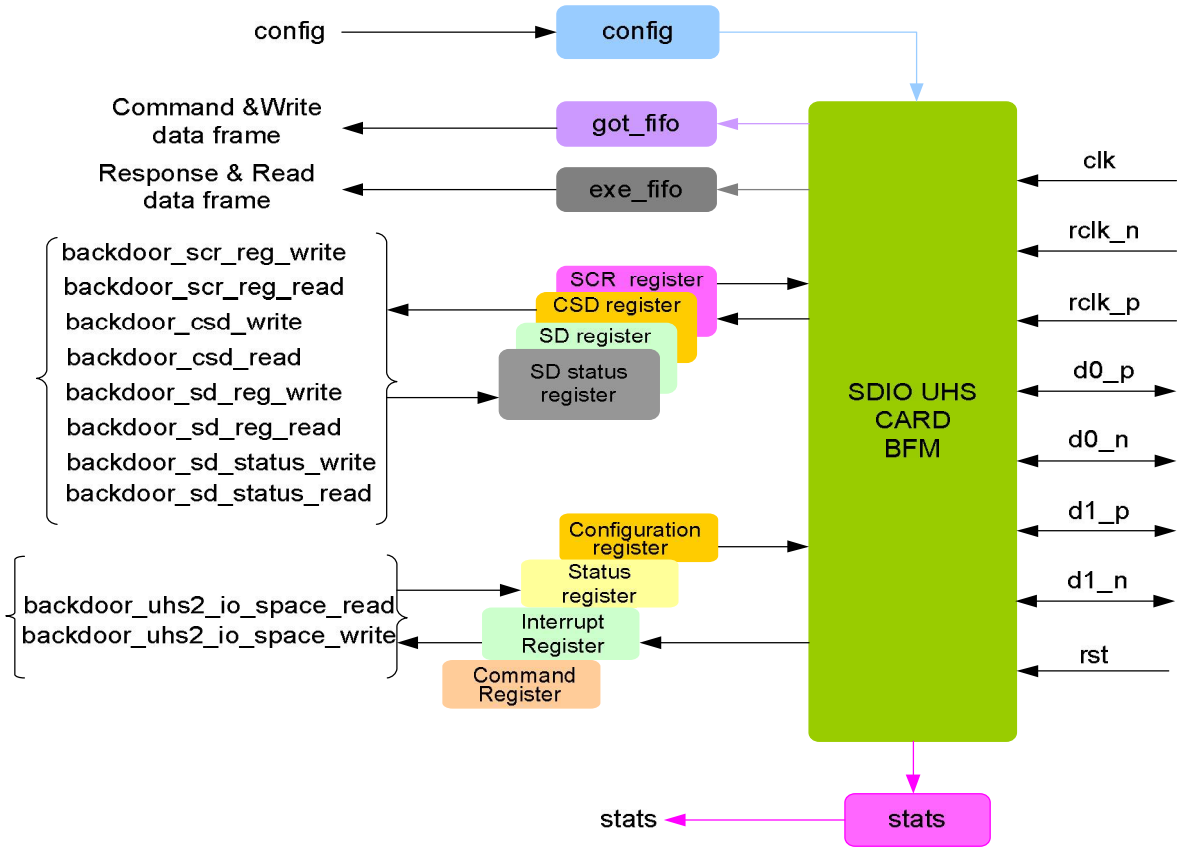


Internal Diagram of UHS-II



SDIO UHS-II Host BFM is first configured with various configuration parameters like read data delay, write data delay, command to command delay, and FIFO depth. User has access to rich set of SDIO UHS-II commands to generate various types of accesses on the SDIO UHS-II bus; these commands are flexible to allow full randomization of various fields of the command. For commands that get response from the card, they are placed in HOST response FIFO. Status counters are updated at the end of transmission of command. Error injection is supported by forcing the host to abort the transfer at the specified position

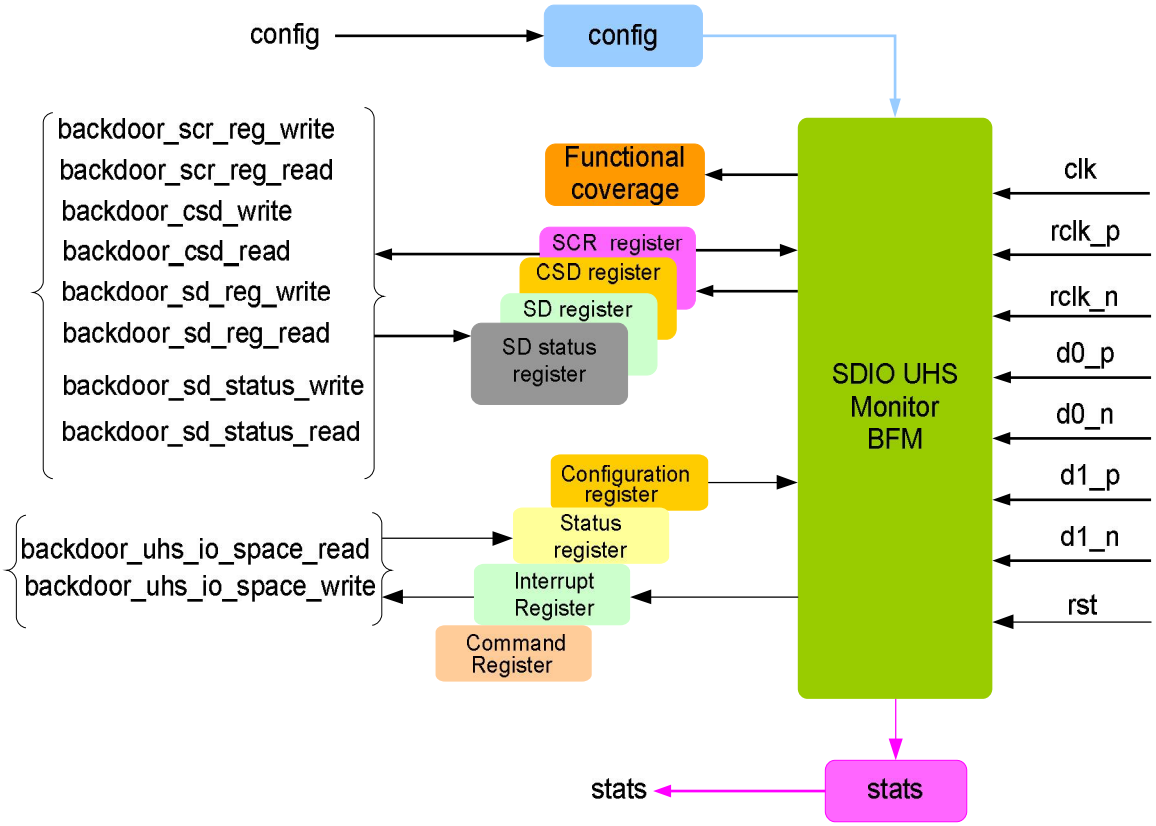
Card Behavior



SDIO UHS-II card is first configured with different configuration parameters. The slave keeps monitoring the bus for a valid command from the host. Depending on command type slave responds to the HOST. For a write command, slave receives data from host and writes to internal memory model. For the read command, slave sends the data to host from the memory model or FIFO. Slave BFM behaves as per the device configured. At the end of command reception, status counters are updated.

Monitor Behavior

Monitor is first configured with different configuration. Monitor monitors the SDIO UHS- II bus for protocol errors and timing errors. Monitor also keeps track of all the accesses on the bus and updates the status counters. These status counters can be accessed any time during simulation. The monitor also implements functional coverage points which user can use to measure the quality of verification.



Supported Simulators

- VCS
- NC-Sim
- Modelsim
- Questasim

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