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# Serial Flash Verification IP

Datasheet September 2011 – Version 1.00

# Overview

The process of verification is getting complex with every passing year; this is due to the fact that complexities of chips are increasing. With such an increasing design complexity, verification tends to consume up to 60-80% project resources and often represents a bottleneck. Having all these in mind, SmartDV has developed number of Verification IP's, which has been created by verification engineers with decades of experience in verifying complex chips.

The SmartDV Verification IP (VIP) for Serial Flash provides an efficient and simple way to verify the Serial Flash master or slave device. The Smart DV VIP for Serial Flash is fully compliant with WINBOND,MICRONIC, SPANSION and Silicon Storage technology(SST) and provides the following features:

- The model has a rich set of configuration parameters to control Serial Flash functionality.
- In slave mode, Serial Flash supports some of the common device models behavior.

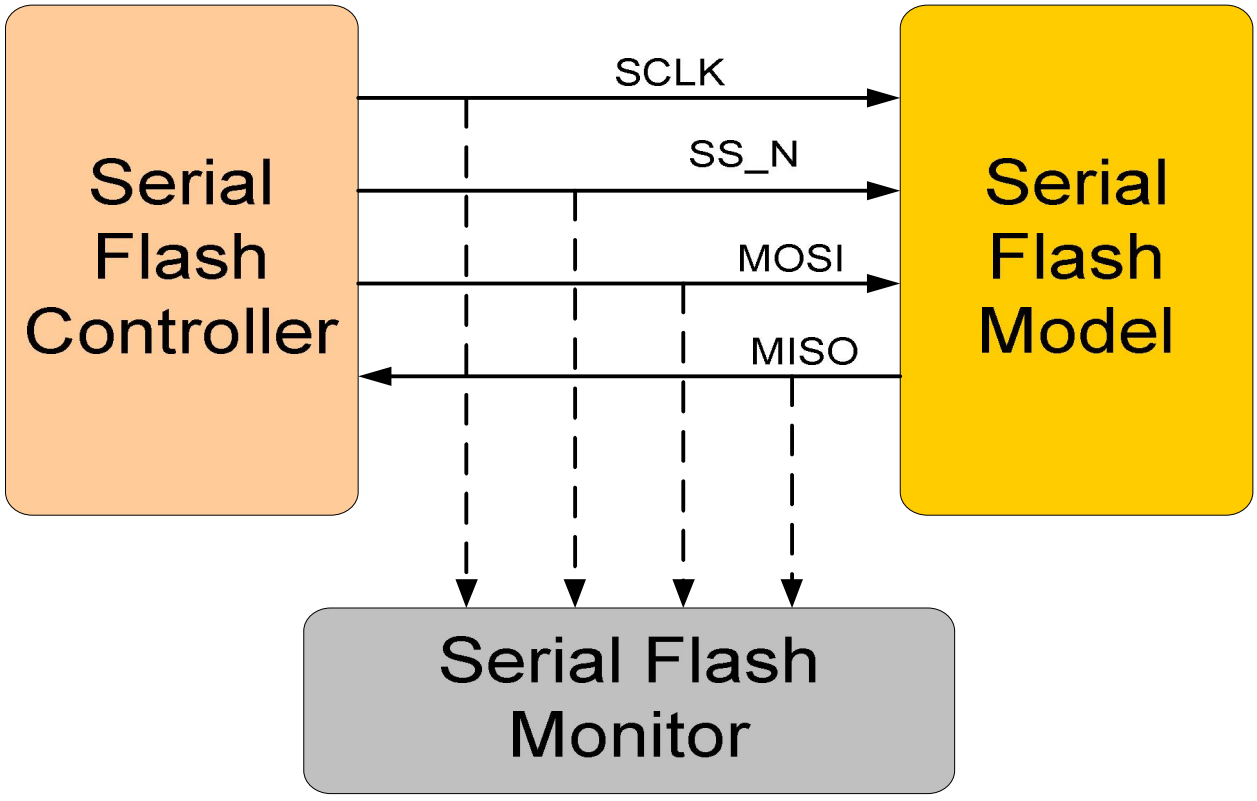
# Features

- Implemented in **Unencrypted OpenVera, Verilog, E, SystemC and SystemVerilog**. Supported RVM, AVM, VMM, OVM, UVM and non-standard verify env.
- Follows Serial Flash specification as defined in WINBOND,MICRONIC, SPANSION, Silicon Storage technology(SST) and many more.
- Supports 3-wire,4-wire interface
- Supports baud rate selection
- Supports internal clock division check.
- Supports on the fly generation of data.
- Supports backdoor initialization of data.
- Supports constraints Randomization.
- Built in functional coverage analysis.
- Supports Callbacks in controller, memory model and monitor for modifying, and sampling data/cmd on bus.
- Notifies the test bench of significant events such as transactions, warnings, and protocol violations. This can be written to separate log files.
- Serial Flash Verification IP comes with **complete testsuite** to test every feature of Serial Flash specification.

# Benefits

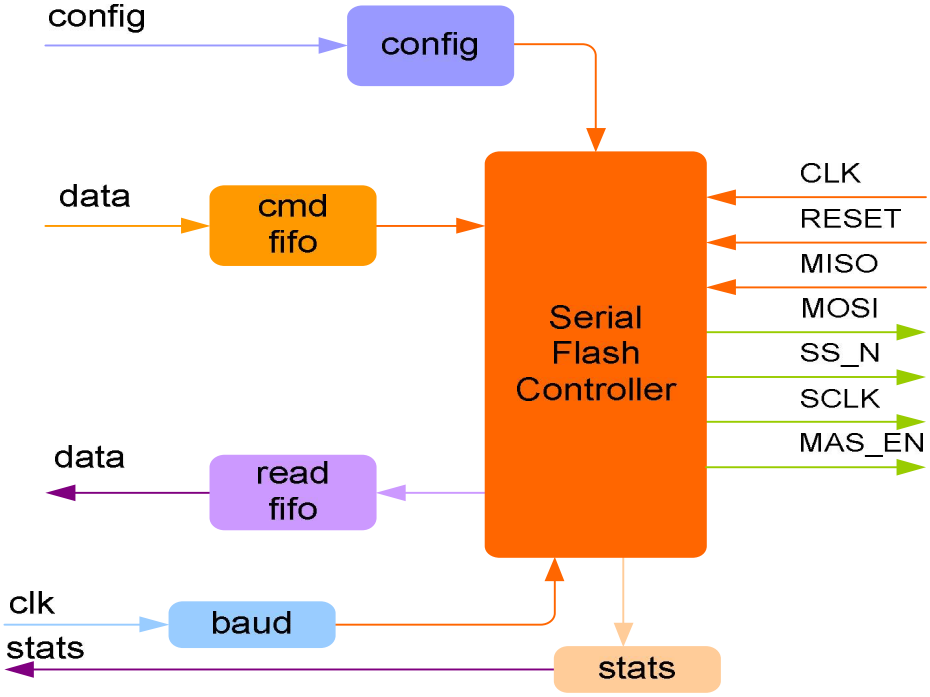
- Faster testbench development and more complete verification of Serial Flash designs.
- Easy to use command interface simplifies testbench control and configuration of slave and master.
- Simplifies results analysis.
- Integrates easily into **OpenVera, SytemVerilog, Specman E, and SystemC**
- Runs in every major simulation environment

# Serial Flash Verification IP Topology



# Master Behavior

Serial Flash VIP master is first configured with different configuration parameters. Parameters like Baud rate, Device Mode. Once configuration is completed, user can use rich set of commands to issue transactions on Serial Flash bus.



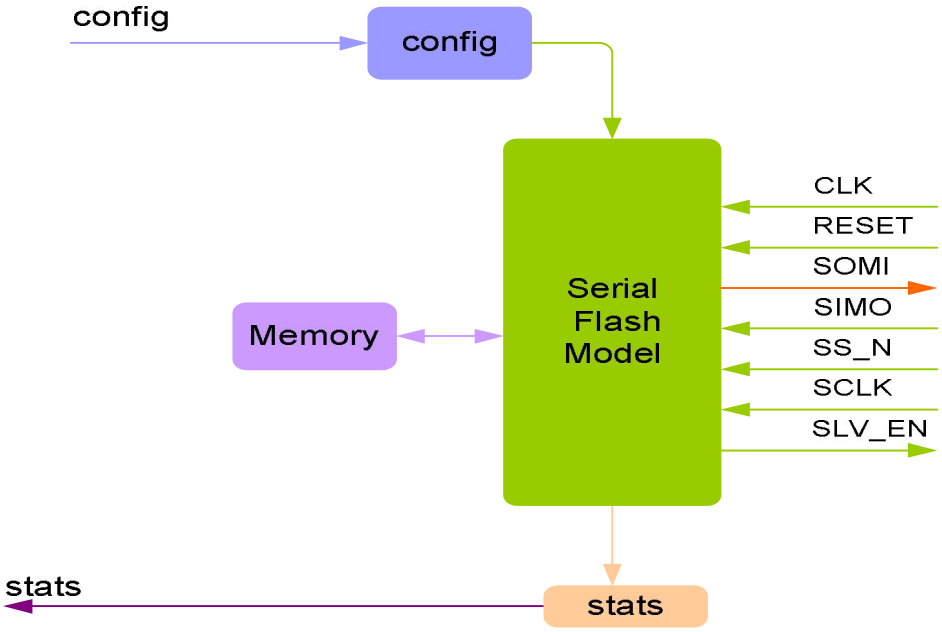

When mode is set to FIFO mode, user needs to use command write (slaveid,data) to write data, read(slaveid) to do read operation, write_read(slaveid,data) to do read/write at same time.

Master BFM supports user callbacks for read and write command processing.

# Slave Behavior

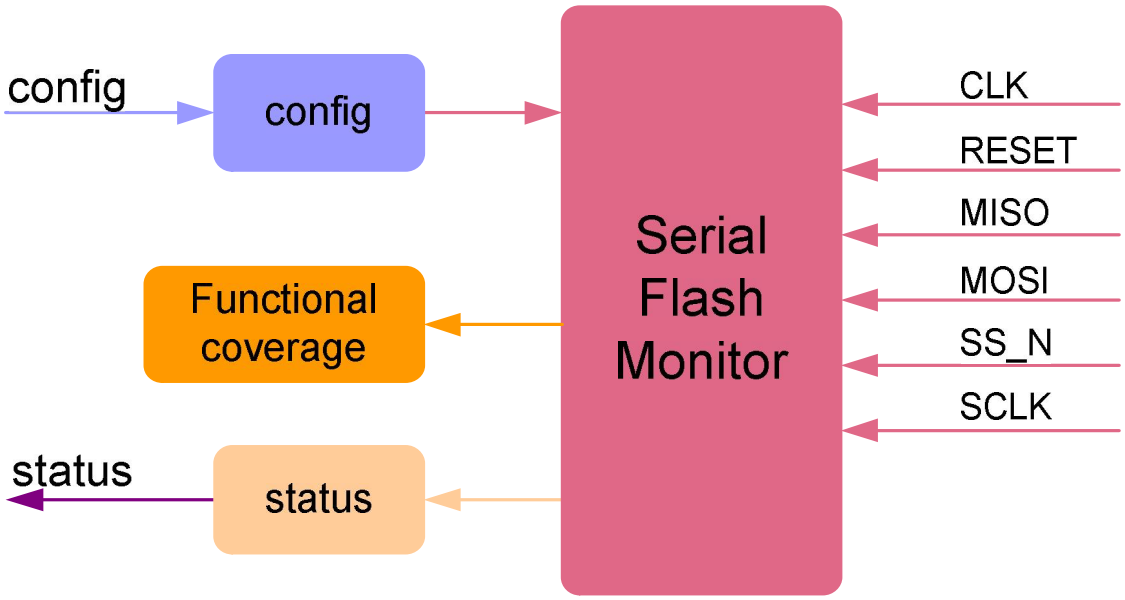
Serial Flash VIP slave is first configured with different configuration parameters. Device Mode Model Mode. Once configuration is completed, Serial Flash VIP slave can respond to transaction on Serial Flash bus.

Serial Flash VIP slave device monitors the bus to determine if it has been selected for a transfer request. It will respond to a transfer request if it has been selected.




# Monitor Behavior

Monitor is first configured with different configuration parameters. A monitor monitors the Serial Flash bus for protocol errors and timing errors. Monitor also keeps track of all the access on bus and these stats can be accessed any time during simulation. Monitor supports user callbacks for read and writes data.




All the access on the bus can be written to log files for post processing.

# Supported Simulators

- VCS
- NC-SIM
- ModelSim
- Questasim

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