MIPI SLIMbus Verification IP

Datasheet October 2011 – Version 1.01.01

Overview

The process of verification is getting complex every year. This is due to the fact that complexities of chips are increasing. With such an increase in design complexity, verification tends to consume up to 60-80% project resources and often represents a bottleneck. Having all these in mind, SmartDV has developed number of Verification IP's which has been created by verification engineers with decades of experience in verifying complex chips.

The SmartDV Verification IP (VIP) for MIPI SLIMbus provides an efficient and simple way to verify the MIPI SLIMbus protocol. The SmartDV VIP for MIPI SLIMbus is fully compliant with version 1.01.01 of the MIPI SLIMbus Specification and provides the following features:

- The model has a rich set of configuration parameters to control MIPI SLIMbus functionality.
- Ability to detect and insert various error types.

Features

- Implemented in **Unencrypted OpenVera, Verilog, E, SystemC and System Verilog.**
- Supported RVM, AVM, VMM, OVM, UVM and non-standard verify env.
- Supports 1.01.01 MIPI SLIMbus specification.
- Organized TDM frame structure allows SLIMbus to carry Control and Data information.
- Provides bi-directional DATA line and unidirectional CLK line.
- Enumeration for device is supported.
- Provides Arbitration mechanism to access the port.
- Provides limited retransmission of Messages.
- Supports Frame layer to interleave Control space and data space in a Sub frame.
- Ports make use of Isochronous, Pushed, Pulled and Asynchronous Protocols.
- Supports all Core Message types.
- User Defined protocol is supported.
- Supports Flow control mechanism.
- Supports Collision Detection for Message channel as well as for Data channel.
- Supports error injection and error detection.

- Supports various Error Management mechanisms.
  - Error on Segments.
  - Framing error.
  - Parity error.
  - Messaging error.
  - Error on Synchronization.
  - CRC error.
- Supports Constraints Randomization.
- Supports Callback for the user to process the data and errors in BFM and Monitor.
- MIPI SLIMbus verification IP comes with complete test suite to test every feature of MIPI SLIMbus specification.
- Functional coverage support for MIPI SLIMbus features.

Benefits

- Faster test bench development and more complete verification of MIPI SLIMbus designs.
- Simplifies result analysis.
- Integrates easily into **OpenVera, SystemVerilog, Specman E, and SystemC**.
- Runs in every major simulation environment.

MIPI SLIMbus Verification IP Topology
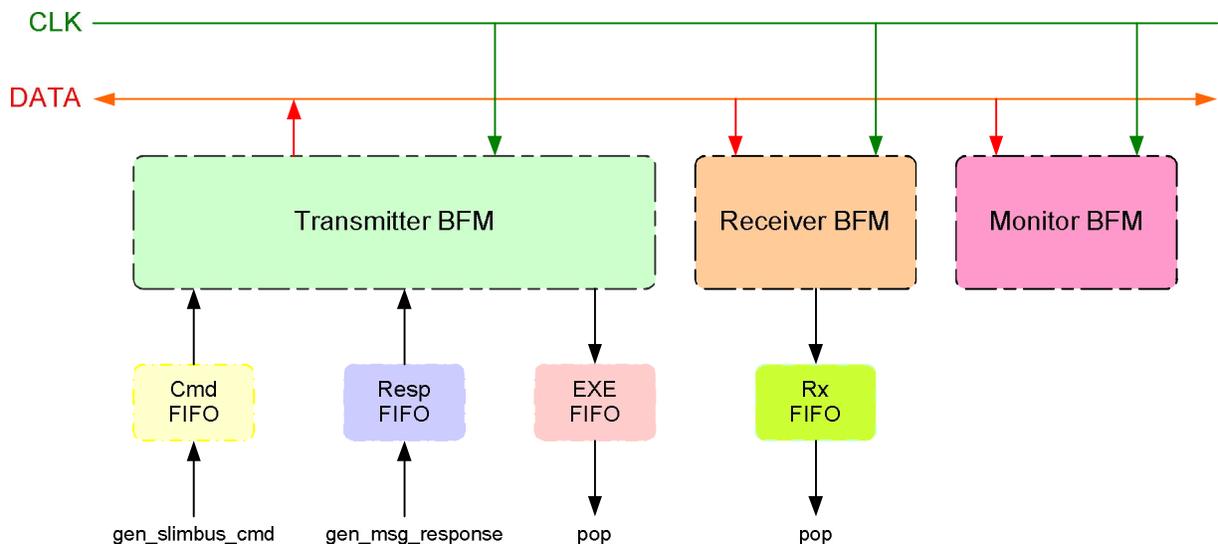
Transmitter Behavior

MIPI SLIMbus Transmitter is first configured with different configuration parameters. These configuration parameters are stored in config object. MIPI SLIMbus BFM initiates the possible frames based on various MIPI SLIMbus commands from the test bench. User uses rich set of methods for sending frames on Transmitter path of BFM. After sending each frame, callbacks are executed to provide control to the user to process the data. At the end of frame transmission status counters are updated.
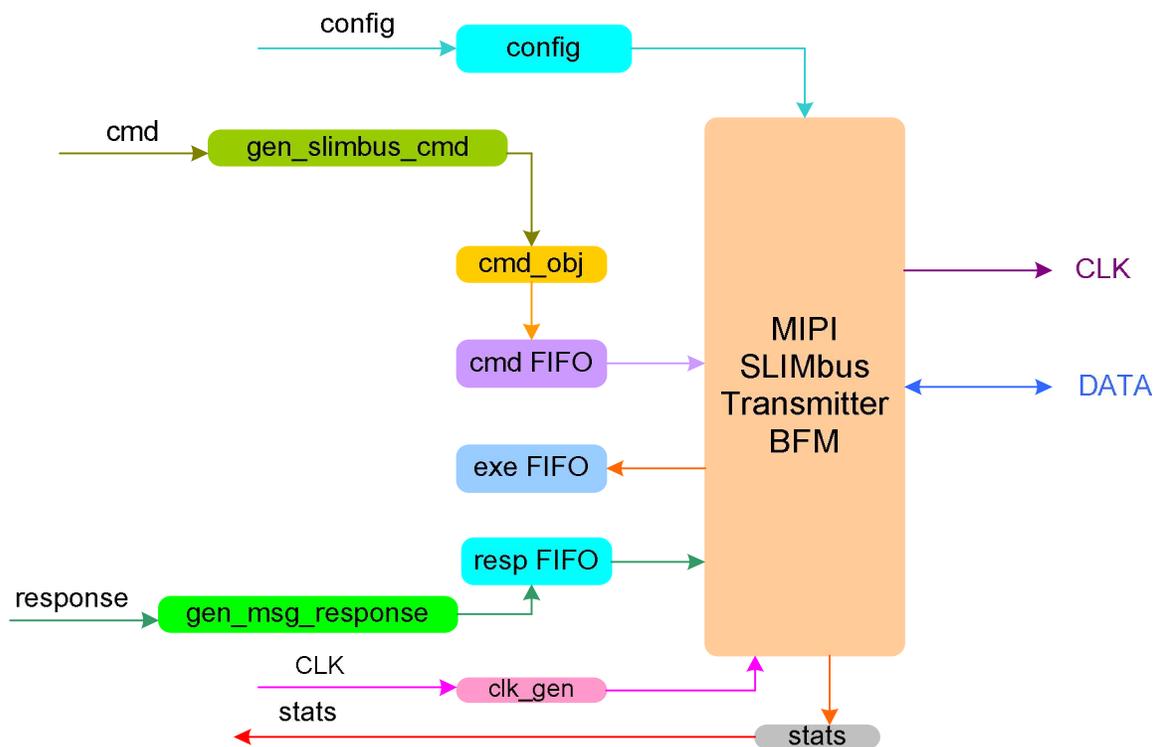

Receiver Behavior

MIPI SLIMbus receiver is first configured with different configuration parameters. These configuration parameters are stored in config object. Receiver device monitors the bus to determine the data transmission. After the collection of each frame, callbacks are used to provide control to the user to process the frame. Status counters are updated once the frame reception is over.
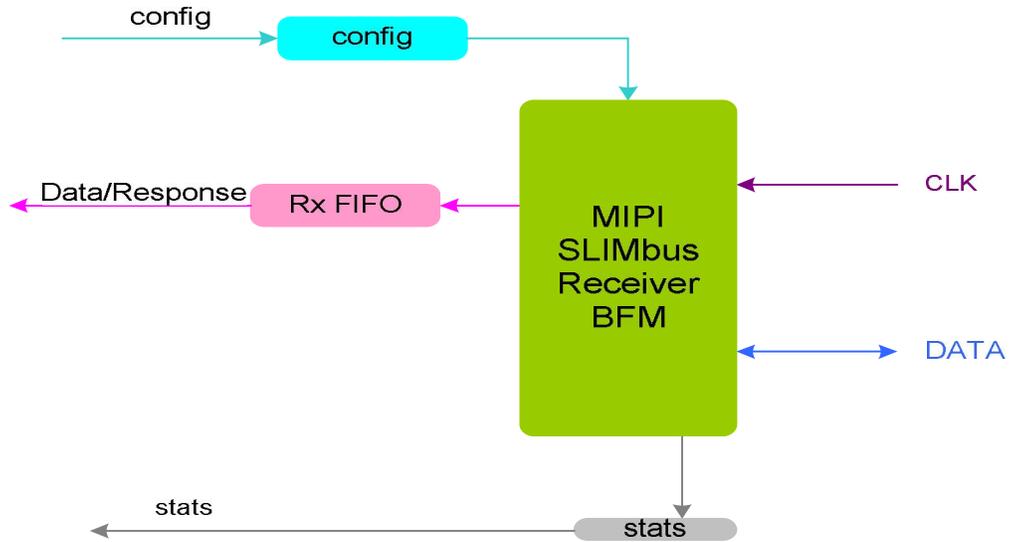
Monitor Behavior

Monitor is first configured with different configuration parameters. A monitor monitors the MIPI SLIMbus for protocol errors and timing errors. Monitor also keeps tracking all the accesses on the bus, updates the status counters. These statuses can be accessed any time during simulation.
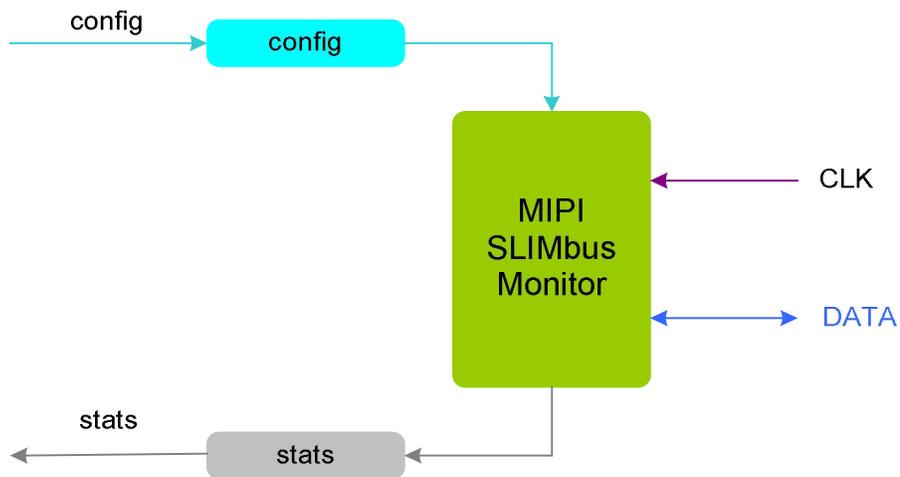
Supported Simulators

- VCS
- NC-SIM
- ModelSim
- Questasim

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