Smart DV Technologies
14/B, 2nd Cross, SR Layout,
Bangalore, India : 560017
E-Mail : info@smart-dv.com
http://www.smart-dv.com

SMBus Verification IP

Datasheet August 2007 – Version 1.0

Overview

The process of verification is getting complex with every passing year; this is due to the fact that complexity of chips are increasing. With such an increasing design complexity, verification tends to consume up to 60-80% project resources and often represents a bottleneck. Having all this in mind, SmartDV has developed number of Verification IP's, which has been created by verification engineers with decades of experience in verifying complex chips.

The SmartDV Verification IP (VIP) for SMbus provides an efficient and simple way to verify the SMBus bidirectional two-wire bus. The SmartDV VIP for SMBus is fully compliant with version 2.0 of the SMBus Bus Specification and provides following features:

- Operates as a Master, Slave. As a Master, the model can Start/Stop all possible transfers. In addition, as a Slave device it can detect Start/Stop conditions and perform data transfers according to the initiator request.
- Supports all speed operations. The model has a rich set of configuration parameters to set clock synchronization and generation of the Serial Clock Line (SMBCLK) to meet all clocking requirements.

Features

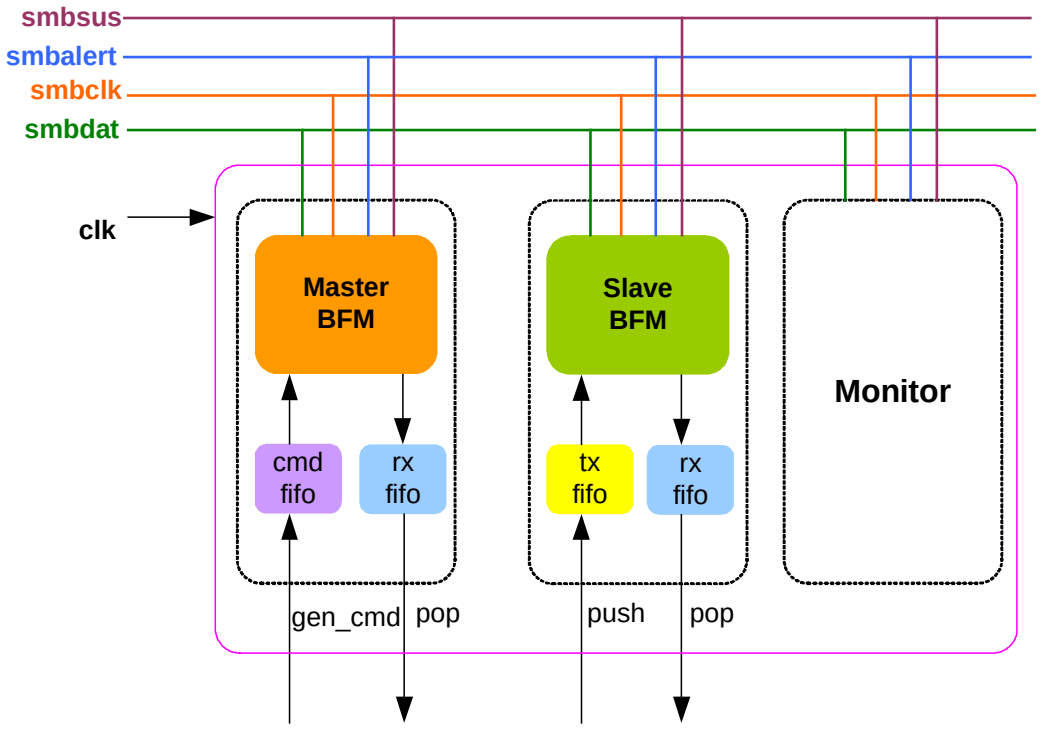
- Implemented in **Unencrypted OpenVera and SystemVerilog**.
- Supported RVM, AVM, VMM and non-standard verify env.
- Full SMBus Master and Slave functionality.
- Supports all the SMBus commands as per the specs.
- Supports programmable clock frequency of operation.
- Support ARP command generation and response.
- Support Timeout detection and generation.
- Bus-accurate timing.
- PEC support
- Supports master/slave arbitration and clock synchronization.
- Glitch insertion and detection.
- Callbacks in master, slave and monitor for user processing of data
- Supports insertion of errors
    - Master abort in middle of transaction.
    - ACK on last read phase by master.
    - Master continues on NACK after write NACK from slave.
    - Random and Periodic clock period stretching by slave.
    - Random Write NACK insertion by slave.

    - PEC Error.
    - Glitch insertion.
    - Timeout error insertion.
- Notifies the testbench of significant events such as transactions, warnings, timing and protocol violations.
- SMBus Verification IP comes with **complete testsuite** to test every feature of SMBus specification.

Benefits

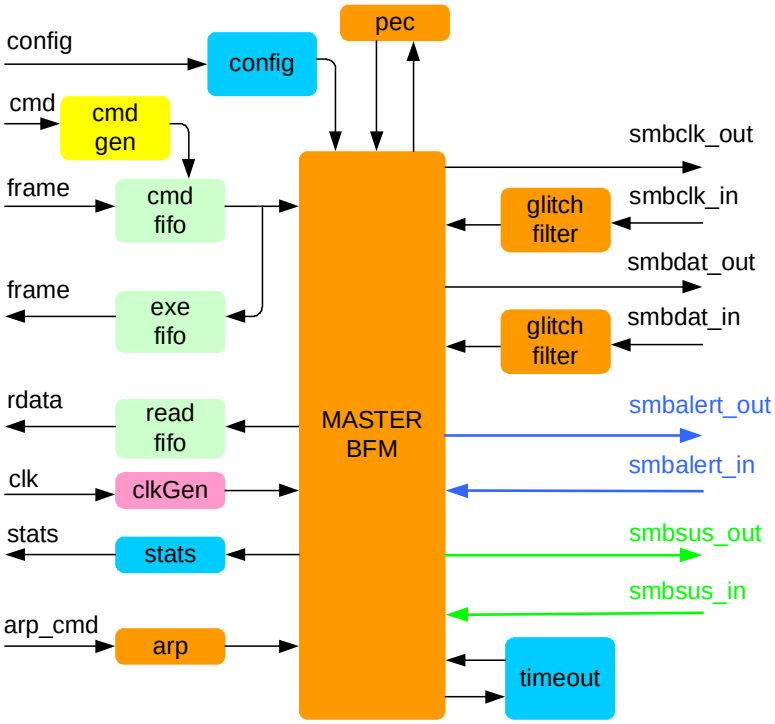
- Faster testbench development and more complete verification of SMBus designs.
- Simplifies results analysis.
- Integrates easily into **OpenVera, SytemVerilog**
- Runs in every major simulation environment

SMBus Verification IP Topology



Master Behavior

Each master is first configured with different configuration parameters. Master then initiates requests based on various SMBus Commands and general call transfers from the testbench. Read data from slave is placed in RX Byte Fifo. The master also arbitrates the bus using the serial data (SMBDAT) and SMBCLK lines and can be configured to react in different ways if the bus is not free. Arbitration follows the rules set by the SMBus protocol.



Master supports following commands for generating access on Smbus.

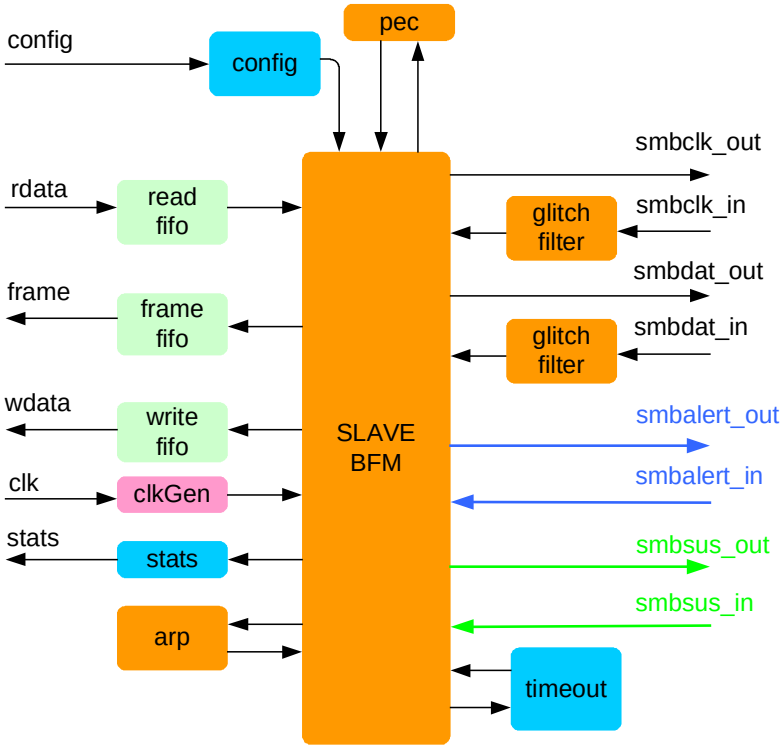
- gen_smbus_quick_cmd
- gen_smbus_send_byte_cmd
- gen_smbus_receive_byte_cmd
- gen_smbus_write_byte_cmd
- gen_smbus_write_word_cmd
- gen_smbus_notify_arp_master_cmd
- gen_smbus_read_byte_cmd
- gen_smbus_read_word_cmd
- gen_smbus_process_call_cmd
- gen_smbus_write_block_cmd
- gen_smbus_read_block_cmd
- gen_smbus_block_write_block_read_process_call_cmd.

For doing random command generation, master supports generic method "**gen_smbus_cmd**". Which user can use to generate all the commands listed above.

Master supports callbacks for user to modify default master behavior. This can be used for NACKing read data, or corrupting PEC. Callbacks can also be used for getting the complete data object at the end of every transfer.

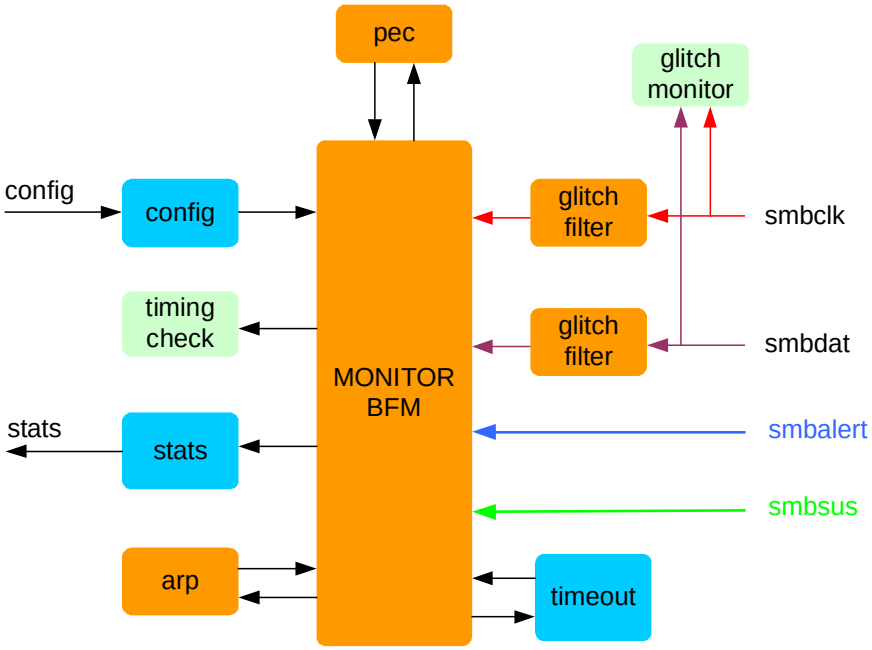
Slave Behavior

Each slave is first configured with different configuration parameters. A slave device monitors the bus to determine if it has been selected (If address matches) for a transfer request. It will always respond to a transfer request if it has been selected. The slave responds to read requests by sending data which can be fed through its TX Byte Fifo. For write requests, the slave receives data transmitted by the master and passes it to the RX Byte fifo. The slave can be made to act erroneously by forcing it to respond with an acknowledgment (or no acknowledgment) to transfer requests. Slave BFM supports user callbacks for read and write command processing. Thus allowing to build any kind of application using callbacks.



Monitor Behavior

Monitor is first configured with different configuration parameters. A monitor monitors the SMBus bus for protocol errors and timing errors. Monitor also keeps track of all the access on bus, and these stats can be accessed any time during simulation.



Monitor like slave and master supports callbacks, this can be used for getting pointer to complete data object for post processing.

Supported Simulators

- VCS
- NC-Sim
- ModelSim
- Nusym

Smart DV Technologies
14/B, 2nd Cross, SR Layout,
Bangalore, India : 560017
E-Mail : info@smart-dv.com
http://www.smart-dv.com