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SpaceWire Verification IP

Datasheet February 2012

Overview

The process of verification is getting complex with every passing year; this is due to the fact that complexities of chips are increasing. With such an increasing design complexity, verification tends to consume up to 60-80% project resources and often represents a bottleneck. Having all this in mind, SmartDV has developed number of Verification IP's, which has been created by verification engineers with decades of experience in verifying complex chips.

The SmartDV Verification IP (VIP) for SpaceWire provides an efficient and simple way to verify the SpaceWire protocol. The SmartDV VIP for SpaceWire is fully compliant with ECSS E-ST-50-12C Standard and provides the following features:

- The model has a rich set of configuration parameters to control SpaceWire functionality.
- Ability to detect and insert various types of error.

Features

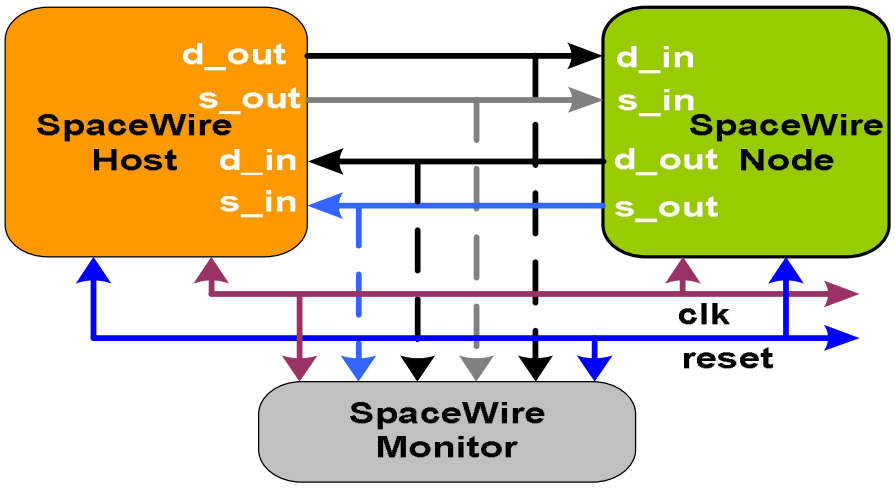
- Implemented natively in OpenVera, Verilog, SystemC, Specman E and SystemVerilog.
- Supported RVM, AVM, VMM, OVM, UVM and non-standard verify env.
- Compliant with ECSS E-ST-50-12C Standard.
- Supports speeds between 2 Mb/s and 400 Mb/s.
- Supports sending packets of information from a source node to a specified destination node
- Supports full-duplex point-to-point serial data communication links.
- Supports Data-Strobe (DS) encoding.
- Support Encoding/Decoding Link interface.
- Support Flow control and link Initialization.
- Includes Time-Codes support.
- Supports all types of errors insertion/detection as given below:
  Link Errors
  - Disconnect error
  - Parity error
  - Escape sequence error
  - Character sequence error
  - Credit error

    - Empty packet error
  - Network Errors
    - Link error
    - EEP received
    - Destination address error
- Provides Link error recovery
- Supports Exchange of silence error recovery procedure.
- Arbitration schemes supported:
    - Priority based
    - Round-robin
    - Random arbitration
    - First come first served
- On-the-fly protocol and data checking.
- Notifies the test bench of significant events such as transactions, warnings, and protocol violations.
- Status counters for various events on bus.
- Callbacks in Host and Node for various events
- Built in functional coverage analysis.
- SpaceWire Verification IP comes with **complete testsuite** to verify each and every feature of SpaceWire specification.

Benefits

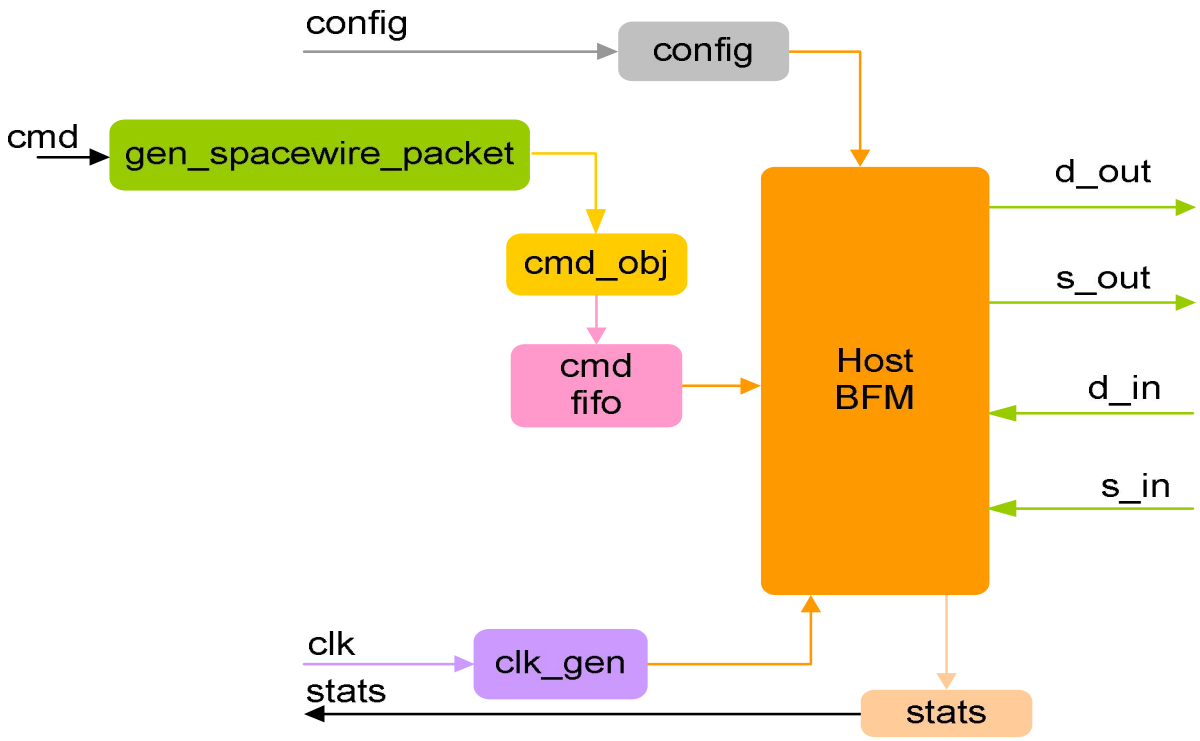
- Faster testbench development and more complete verification of SpaceWire designs.
- Easy to use command interface simplifies test bench control and configuration of Host and Node.
- Simplifies results analysis.
- Runs in every major simulation environment

SpaceWire Verification IP Topology



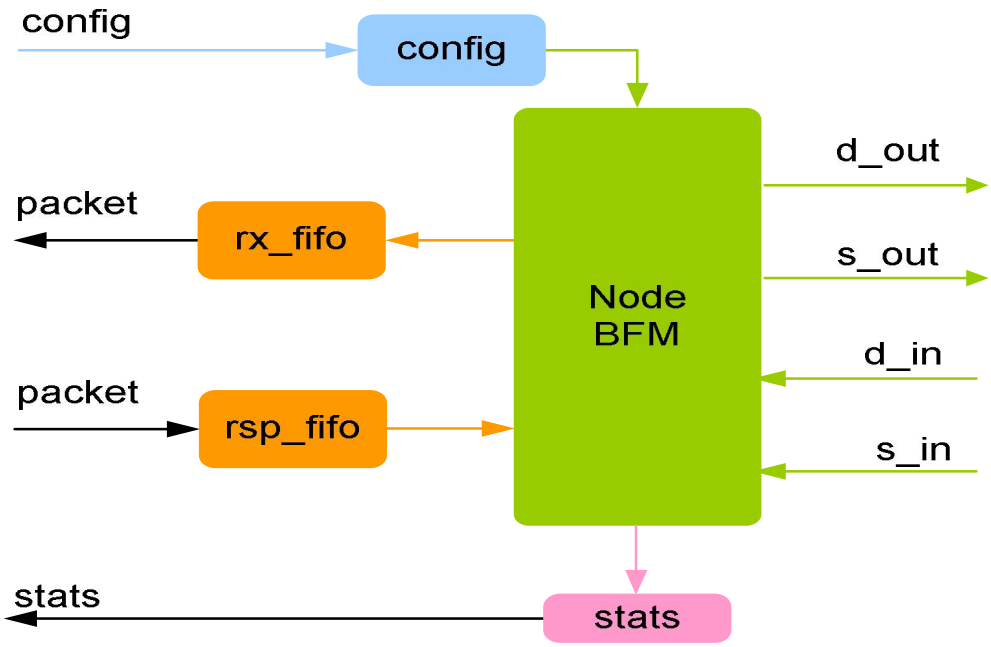
Host Behavior

SpaceWire VIP host is first configured with different configuration parameters. The host system for holding data prior to transmission through a link interface. The host transmitter then initiates request based commands from the test cases. The host transmitter is responsible for encoding data and transmitting it using DS encoding technique. It receives packets for transmission. It supports to injection of various Link errors. At the end of transmitting each packet transmission stats are updated.



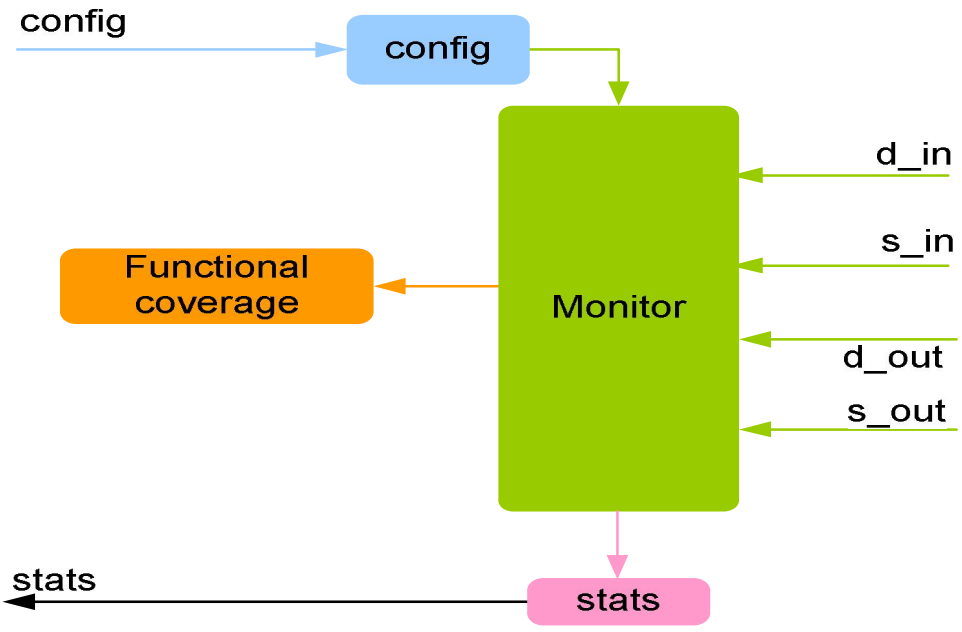
Node Behavior

SpaceWire VIP node is first configured with different configuration parameters. SpaceWire node shall accept a stream of packets from the host system for transmission or provides a stream of packets to the host system after reception from the SpaceWire link, or do both. The node receiver is also responsible for detection of disconnect, parity, escape and credit errors and it flags these errors to the state machine. At each stage of the Node receive FSM, callbacks are executed and user can use these callbacks to modify the behavior of the FSM.



Monitor Behavior

Monitor is first configured with different configuration parameters. A monitor monitors the bus for protocol errors and timing errors. Monitor also keeps track of all the accesses on bus and these stats can be accessed any time during simulation. The Monitor also logs all transactions into a file that can be configured through the use of methods. Monitor implements the functional coverage, which user can modify to add more coverage in object oriented way.



Supported Simulators

- VCS
- NC-SIM
- Modelsim
- Questasim

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