Smart DV Technologies India Private Limited
14/B, 2nd Cross, SR Layout,
Bangalore, India : 560017
E-Mail : info@smart-dv.com
http://www.smart-dv.com

SPDIF Verification IP

Datasheet September 2011 – Version 1.0

Overview

The process of verification is getting complex with every passing year; this is due to the fact that complexity of chips are increasing. With such an increasing design complexity, verification tends to consume up to 60-80% project resources and often represents a bottleneck. Having all this in mind, SmartDV has developed number of Verification IP's, which has been created by verification engineers with decades of experience in verifying complex chips.

The SmartDV Verification IP (VIP) for SPDIF provides an efficient and simple way to verify the SPDIF IEC 60958. The SmartDV VIP for SPDIF is fully compliant with Standard SPDIF Specifications IEC 60958 and provides the following features:

- The model has a rich set of configuration parameters to control SPDIF functionality.
- Ability to detect and insert various types of error.
- The transmitter is capable of inserting various transmit errors.
- The receiving is capable of detecting various received errors.

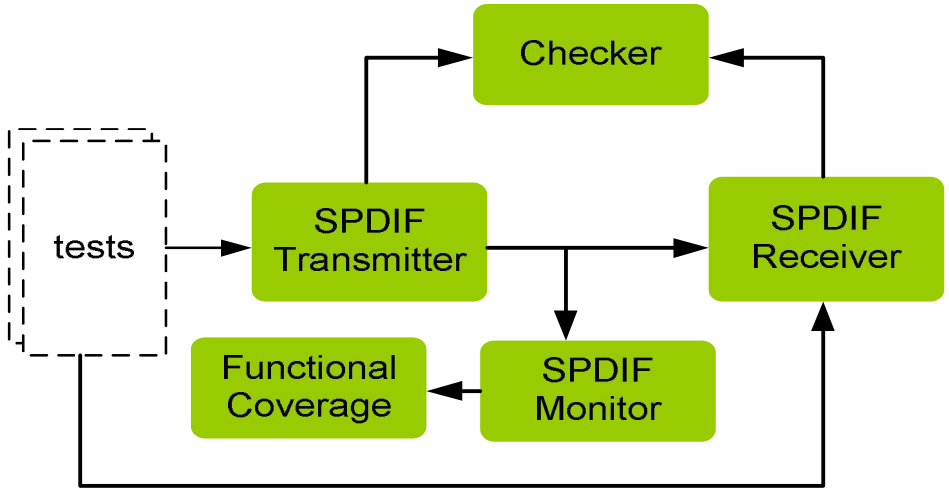
Features

- Implemented in **Unencrypted OpenVera, SystemVerilog, Verilog, SystemC and Specman E.**
- Supported RVM, AVM, VMM, OVM, UVM and non-standard verify env.
- Full SPDIF functionality.
- Configurable Baud rate control.
- Error Injection
  - NRZ encoding error
  - Preamble error
  - Channel encoding error
  - Parity Error
  - Various field errors
- FIFO depth programmable.
- Notifies the testbench of significant events such as transactions, warnings, and protocol violations.
- SPDIF Verification IP comes with **complete testsuite** to verify each and every feature of SPDIF specification.
- Built in functional coverage analysis.

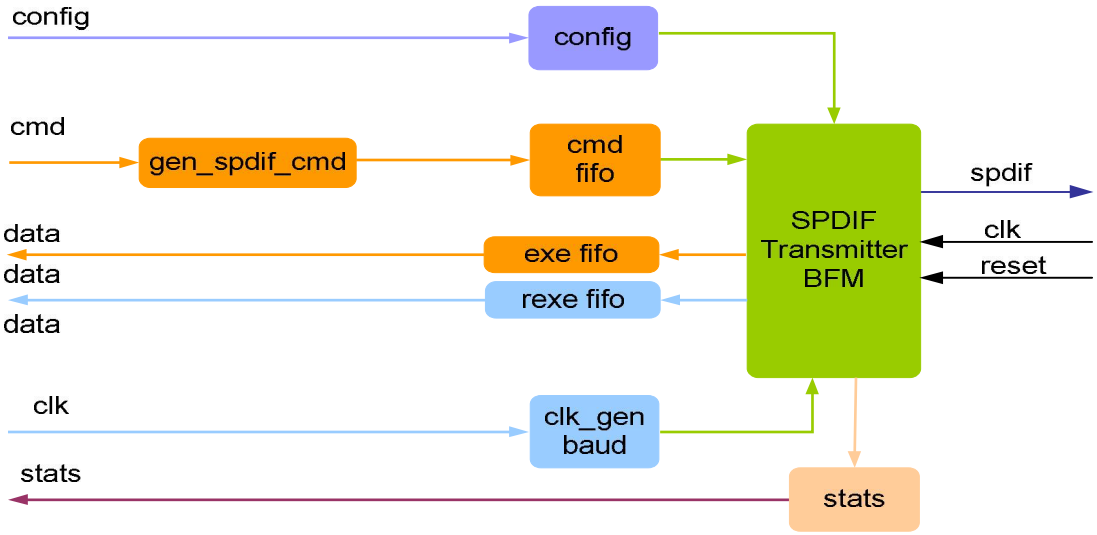
Benefits

- Faster testbench development and more complete verification of SPDIF designs.
- Easy to use command interface simplifies testbench control and configuration of TX and RX
- Simplifies results analysis.
- Runs in every major simulation environment

SPDIF Verification IP Topology



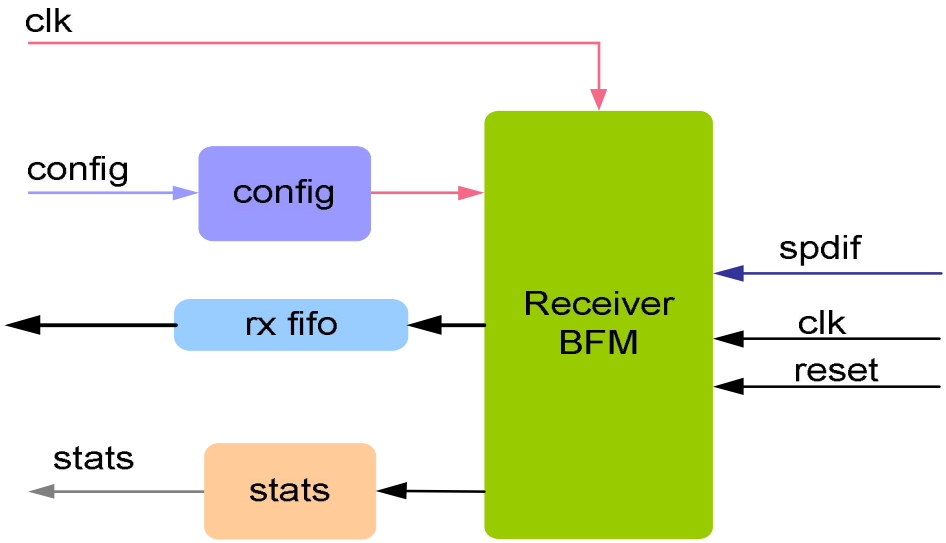
SPDIF Transmitter BFM Behavior



SPDIF verification IP acts as a transmitter. Transmitter is first configured with different configuration parameters. Configuration parameters are baud rate, transmit FIFO depth. Error insertion can be performed for common serial data and frame transmission errors. FIFO's are used to store data transmitted during serial.

At each stage of transmission, callbacks are executed for giving control to user to processing the data being transmitted. Status counters are updated at the end of transmission.

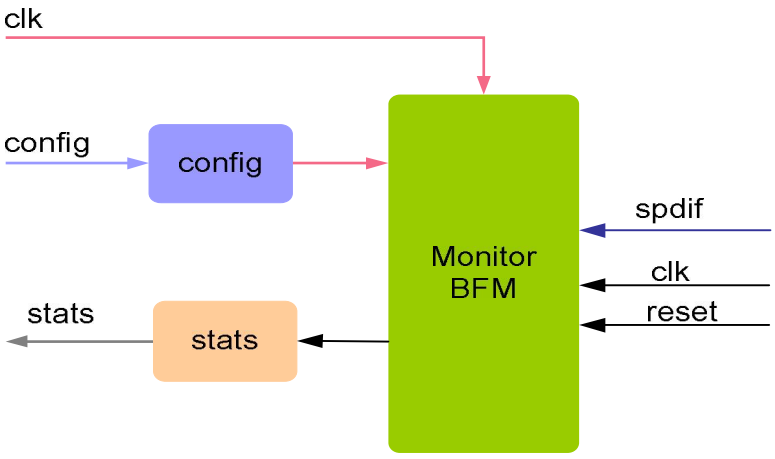
SPDIF Receiver BFM Behavior



SPDIF verification IP acts as a receiver. Receiver is first configured with different configuration parameters. Configuration parameters are baud rate,receive FIFO depth. Receiver recovers the clock from serial data, and samples the frames. Error detections is performed for common serial data and frame transmission errors. FIFO's are used to store data recevied during serial.

At each stage of receiption, callbacks are executed for giving control to user to processing the data being transmitted. Status counters are updated at the end of transmission.

Monitor Behavior



Monitor is first configured with different configuration parameters. A monitor monitors the SPDIF bus, recovers the clock, samples frames. Monitor also keeps track of all the access on bus, and these stats can be accessed any time during simulation. Protocol checking begins after a valid reset, or without a reset if configured for this condition. The Monitor also logs all transactions into a file that can be configured through the use of log methods.

Supported Simulators

- VCS
- NC-SIM
- Modelsim
- Questasim

Smart DV Technologies India Private Limited
14/B, 2nd Cross, SR Layout,
Bangalore, India : 560017
E-Mail : info@smart-dv.com
http://www.smart-dv.com