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UART Verification IP

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Overview

The process of verification is getting complex with every passing year; this is due to the fact that complexities of chips are increasing. With such an increasing design complexity, verification tends to consume up to 60-80% project resources and often represents a bottleneck. Having all this in mind, SmartDV has developed number of Verification IP's, which has been created by verification engineers with decades of experience in verifying complex chips.

The SmartDV Verification IP (VIP) for UART provides an efficient and simple way to verify the UART, RS232 and GPIO. The SmartDV VIP for UART is fully compliant with Standard UART Specification and provides the following features:

- The model has a rich set of configuration parameters to control UART functionality.
- Ability to detect and insert various types of error.
- Contains 16 general-purpose input signals and 16 general-purpose output signals, which can be controlled with read and write commands.
- Configurable for any RS-232 protocol interface in the design.
- Supports IRDA protocol support
- The transmitter is capable of transmitting data of various sizes, with and without parity.
- The transmitter is capable of inserting various transmit errors.
- The receiving is capable of detecting various received errors.

Features

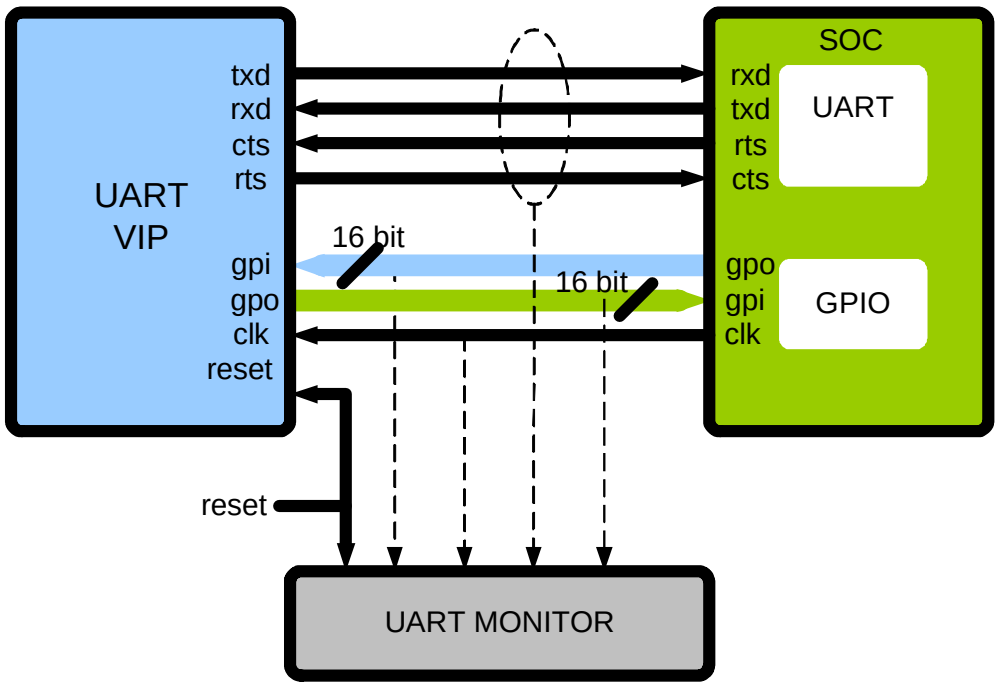
- Implemented in **Unencrypted OpenVera, Verilog, SystemC, SystemVerilog and Specman E.**
- Supported RVM, AVM, VMM, OVM, UVM and non-standard verify env.
- Full UART functionality.
- Support additional functionality of RS232 and GPIO.
- Configurable Baud rate control.
- Full duplex operation.
- Supports character width from 1 bit to 32 bits.
- Supports number of stop bit configuration
- Parity type
  - Even
  - Odd
  - Mark

    - Space
    - No parity
- Error Injection
    - Framing Error
    - Parity Error
- FIFO depth programmable.
- Auto CTS/auto RTS hardware flow control.
- GPIO are supported using read and write commands.
- Supports IRDA protocol.
- Ability to transmit strings to help verification of SOC.
- Notifies the test bench of significant events such as transactions, warnings, and protocol violations.
- UART Verification IP comes with **complete test suite** to verify each and every feature of UART specification.
- Built in functional coverage analysis.

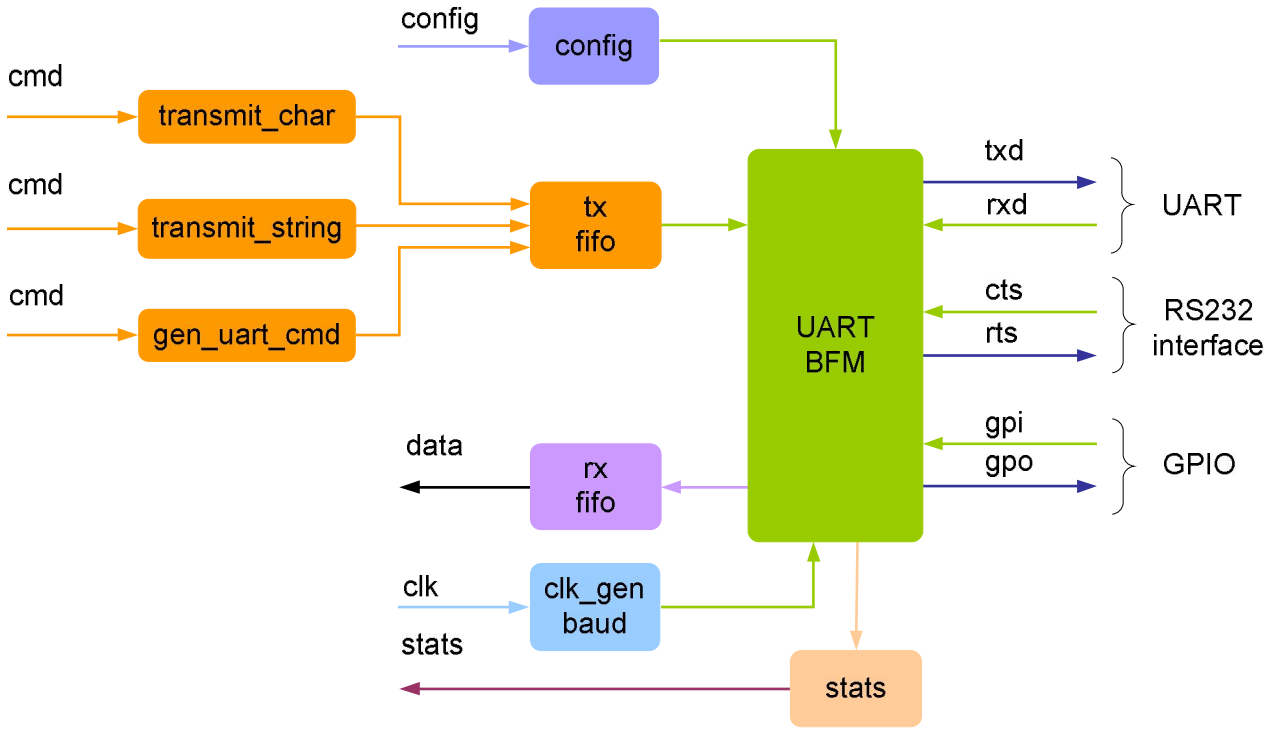
Benefits

- Faster test bench development and more complete verification of UART designs.
- Easy to use command interface simplifies test bench control and configuration of TX and RX.
- Simplifies results analysis.
- Runs in every major simulation environment

UART Verification IP Topology



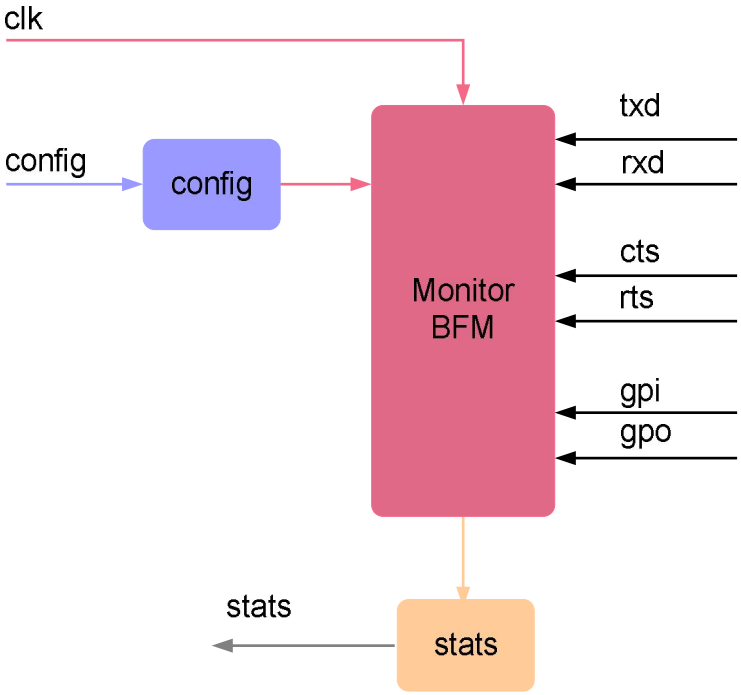
UART BFM Behavior



UART verification IP acts as a transmitter, receiver, with and without RS232 protocol function. Each UART BFM is first configured with different configuration parameters. Configuration parameters are data width, number of stop bits, and type of parity, inter packet delay, inter character gap, mode as UART/RS232, transmit FIFO depth, receive FIFO depth. Error insertion can be performed for common serial data transmission errors. FIFO's are used to store data received and transmitted during serial.

At each stage of transmission and receptions, callbacks are executed for giving control to user to processing the data being transmitted and received. Status counters are updated at the end of transmission and reception.

Monitor Behavior



Monitor is first configured with different configuration parameters. A monitor monitors the UART TXD and RXD for protocol. Monitor also keeps track of all the access on bus, and these stats can be accessed any time during simulation. Protocol checking begins after a valid reset, or without a reset if configured for this condition. The Monitor also logs all transactions into a file that can be configured through the use of log methods. The Monitor has the same configuration parameters as the Transceiver to set up data width, stop bits, and parity bits.

Supported Simulators

- VCS
- NC-SIM
- Modelsim
- Questasim

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