Smart DV Technologies India Private Limited
14/B, 2nd Cross, SR Layout,
Bangalore, India : 560017
E-Mail : info@smart-dv.com
http://www.smart-dv.com

VByOne Verification IP

Datasheet April 2012 – Version 1.4

Overview

The process of verification is getting complex with every passing year; this is due to the fact that complexity of chips is increasing. With such an increasing design complexity, verification tends to consume up to 60-80% project resources and often represents a bottleneck. Having all this in mind, SmartDV has developed number of Verification IP's, which has been created by verification engineers with decades of experience in verifying complex chips.

The SmartDV Verification IP (VIP) for VByOne provides an efficient and simple way to verify VByOne protocol bus. The SmartDV VIP for V-by-One Verification IP is fully compliant with VByOne revision 1.2/1.3 and provides following features:

- Supports VByOne revision 1.2/1.3 specification.
- Operates as RAW/TBI/SERIAL RX/TX and RAW/TBI/SERIAL monitor.

Features

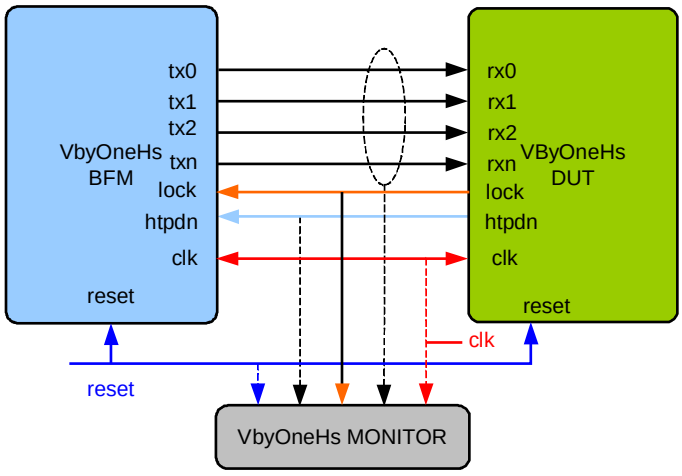
- Supported natively in **Systemverilog, VMM, OVM, UVM, AVM, SystemC, Verilog and Specman E** Languages.
- Follows VByOne specification as 1.2/1.3
- Supports Transmitter and Receiver Mode
- Supports up to 32 lanes
- Supports all byte lengths, color depths, and resolutions
- Supports lane skew insertion in transmitter mode
- Supports disparity and invalid code insertion in 8b/10b.
- Scrambler can be enabled or disabled.
- Supports insertion of scrambler errors.
- Support on the fly generation of data.
- Detects and reports the following errors
  - Invalid control characters injection
  - Invalid data characters injection
  - Invalid 10 bit code injection
  - Disparity errors
  - Alignment errors
- VIP can be connected to DUT at following interfaces
  - Serial interface : txn, txp
  - TBI interface : After 8b/10b Encoder in tx and before 8b/10b decoder in rx
  - Raw Interface : Before 8b/10b Encoder in tx and after 8b/10b decoder in rx

- Functional coverage to cover each and every feature of the VByOne specification
- Test suite to test each and every feature of VByOne specification.
- Callbacks monitor, transmitter and receiver for various events.
- Status counters for various events on bus.

Benefits

- Faster testbench development and more complete verification of VByOne designs.
- Simplifies results analysis.
- Integrates easily into **OpenVera, SytemVerilog, Verilog and SystemC**
- Runs in every major simulation environment.

VByOne Verification IP Topology



VByOne BFM Behavior

VByOne BFM is first configured with different configuration parameters; SmartDV's VByOne verification supports rich set of configuration parameters to control each and every possible configuration parameter. User is provided with rich set of methods to generate different types of frame on the VByOne. After power on transmitter drive HTPDN signal is as low for connect with RX. Rx is wait for CDR(Clock data recovery) training pattern & ALN training pattern.In rx ALN training pattern is finished it will move to normal state.Then TX will pack the data & drive to RX.The RX unpack the data frame after completely received from TX, pushes them to receiver fifo (or channel) Status counter are updated at the end of transmission of frame.

TX BFM supports insertion of various errors, and RX BFM supports detection of all the errors.

VByOne Monitor Behavior

Monitor is first configured with different configuration parameters. A monitor monitors the bus for protocol errors and timing errors. Monitor also keeps track of all the access on bus, updates the status counters.

Monitor also implements functional coverage, which can be used for tracking quality of verification.

Supported Simulators

- VCS
- NC-Sim
- ModelSim
- Questasim

Smart DV Technologies India Private Limited,
14/B, 2nd Cross, SR Layout,
Bangalore, Karnataka,
India - 560017
E-Mail : info@smart-dv.com
http://www.smart-dv.com