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Wishbone Verification IP

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Overview

The process of verification is getting complex with every passing year; this is due to the fact that complexities of chips are increasing. With such an increasing design complexity, verification tends to consume up to 60-80% project resources and often represents a bottleneck. Having all this in mind, SmartDV has developed number of Verification IP's, which has been created by verification engineers with decades of experience in verifying complex chips.

The SmartDV Verification IP (VIP) for Wishbone provides an efficient and simple way to verify the Wishbone. The SmartDV VIP for Wishbone is fully compliant with Wishbone B3 Specification and provides the following features:

- The model has a rich set of configuration parameters to control Wishbone functionality.
- Ability to detect and insert various types of error.

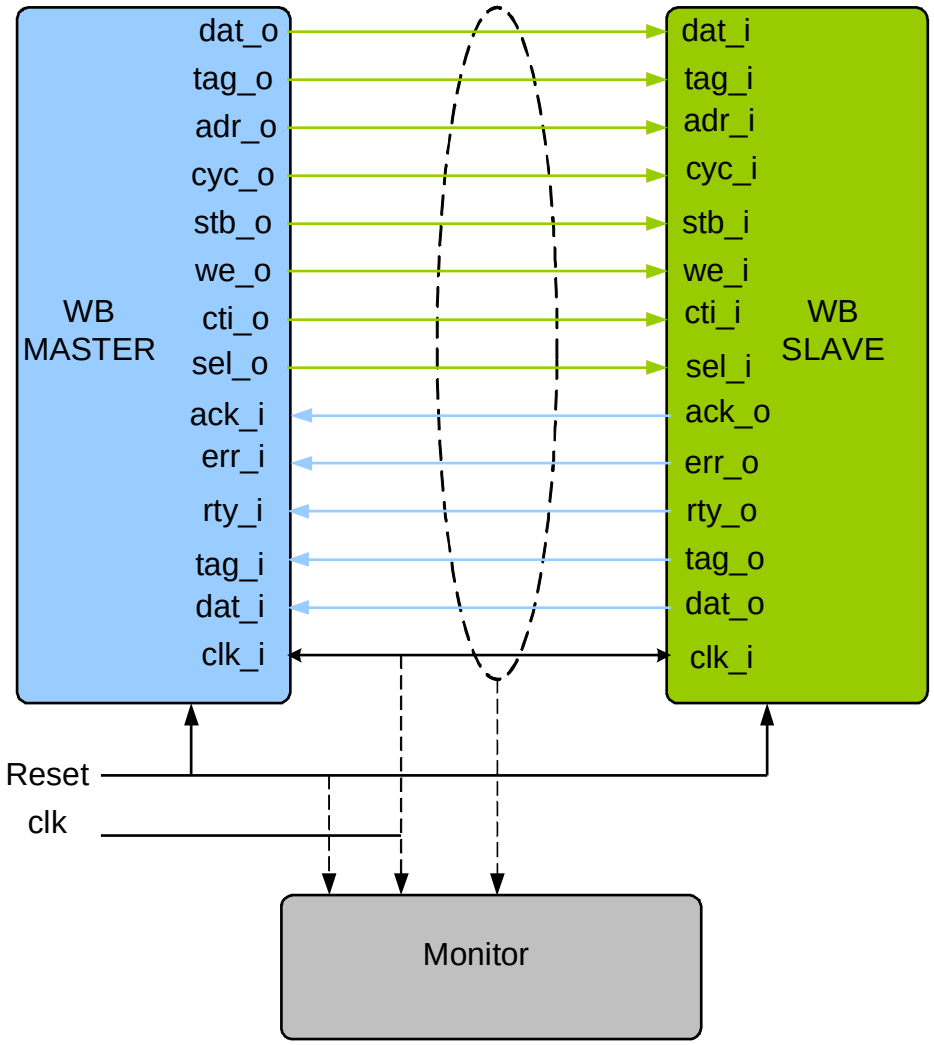
Features

- Implemented in **Unencrypted OpenVera, SystemVerilog, Verilog, SystemC and Specman E.**
- Supported RVM, AVM, VMM, OVM, UVM and non-standard verify env.
- Compliant to OpenCores Wishbone B3 Protocol.
- Support for all types of Wishbone devices
  - Master
  - Slave
- Support for programmable wait states.
- Support for programmable Retry insertion.
- Support for programmable error insertion.
- Configurable transfer size for read and write transactions.
- Support for linear, fixed and wrap burst sizes.
- Ability to inject errors during data transfer.
- Flexibility to send completely configured data.
- On-the-fly protocol and data checking.
- Notifies the testbench of significant events such as transactions, warnings, and protocol violations.
- Wishbone Verification IP comes with **complete testsuite** to verify each and every feature of Wishbone specification.
- Built in functional coverage analysis.

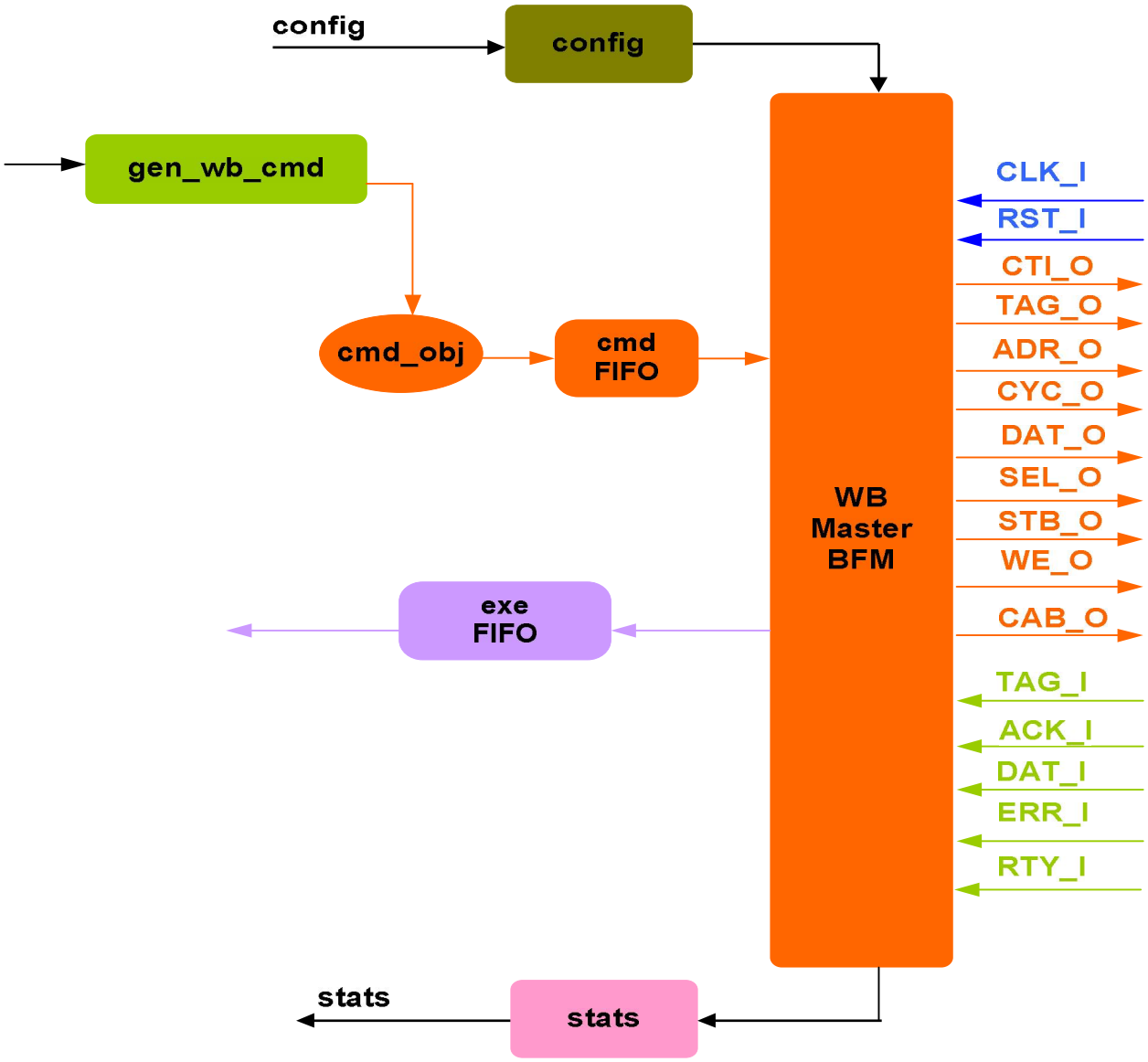
Benefits

- Faster testbench development and more complete verification of OpenCores Wishbone B3 designs.
- Easy to use command interface simplifies testbench control and configuration of master and slave.
- Simplifies results analysis.
- Runs in every major simulation environment

Wishbone Verification IP Topology



Master Behavior

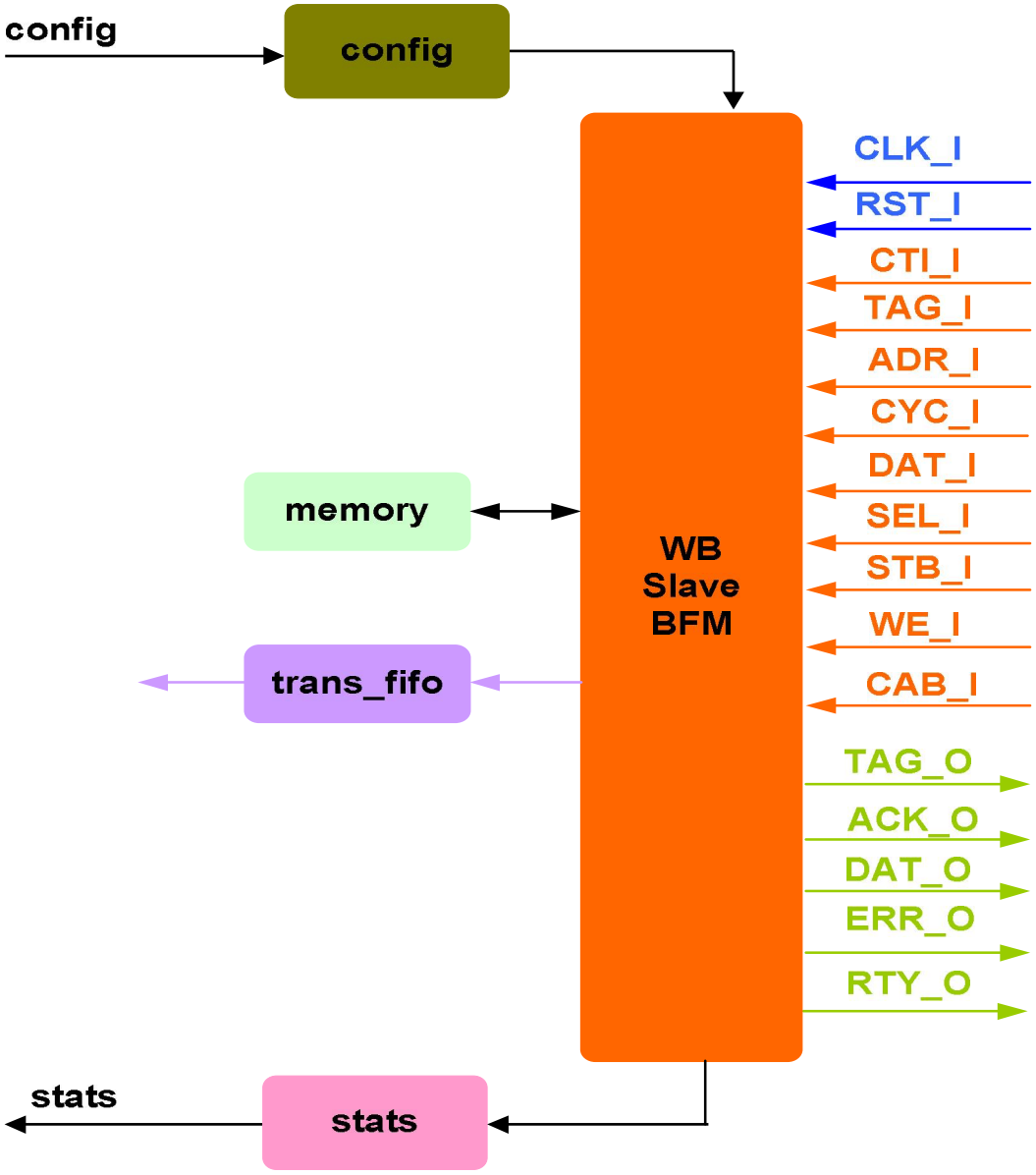


Wishbone master is first configured with different configuration parameters. The master then initiates requests based on read, and write commands from the testcase. In OVM/UVM flow test generates the read and write sequences. Read data from slave is returned in method/sequence which user called. Master implements all the protocols checks and timing checks for checking slaves response.

Master implements callbacks at each stage of internal state machine, user can use this callbacks to change the default behavior of master.

At end of each transaction, stats are updated and also functional coverage is updated. Master also supports transaction dumping to log separate log file which can be used for post processing.

Slave Behavior



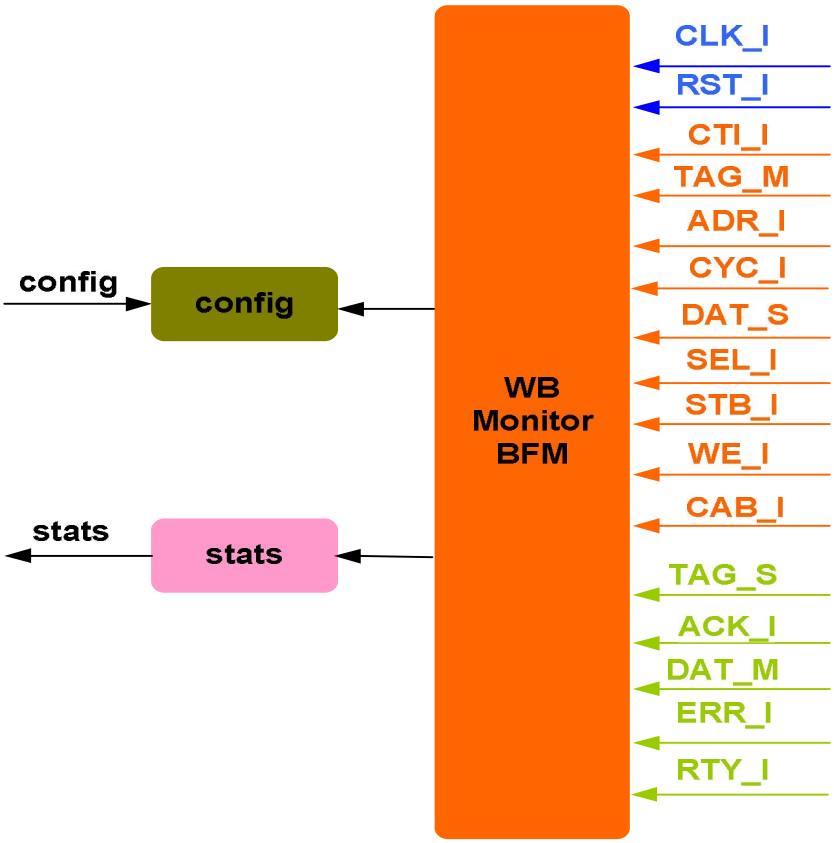
Each slave is first configured with different configuration parameters. A slave device monitors the bus to determine if it has been selected for a transfer request. It will always respond to a transfer request if it has been selected. The slave responds to read requests by sending data which can be fed through its internal memory. For write requests, the slave receives data transmitted by the master and passes it to the internal memory. The slave can be made to act erroneously by forcing it to respond with timeout, or assert Error or assert Retry to transfer

requests.

Slave implements callbacks at each stage of internal state machine, user can use this callbacks to change the default behavior of slave.

At end of each transaction, stats are updated and also functional coverage is updated. Slave also supports transaction dumping to log separate log file which can be used for post processing.

Monitor Behavior



Monitor is first configured with different configuration parameters. A monitor monitors the bus for protocol errors and timing errors. Monitor also keeps track of all the access on bus, and this stats can be accessed any time during simulation. Protocol checking begins after a valid reset, or without a reset if configured for this condition. The Monitor also logs all transactions into a file that can be configured through the use of parameters. The Monitor has the same configuration parameters as the Transceiver to set up.

Supported Simulators

- VCS
- NC-SIM
- ModelSim
- Questasim

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