Cadence SuperSpeed USB 3.0 IP Solution

Configured controller, PHY, verification IP, and driver

Cadence® SuperSpeed USB 3.0 IP is a fully integrated USB 3.0 interface solution, optimized to reduce the cost of integrating and verifying a system on chip (SoC) and the associated embedded software. The solution can contain either a host or device controller, configured to meet the exact functional and integration needs of the system.

Fully integrated solution

A comprehensive hardware/software (HW/SW) verification environment is provided that includes pre-configured verification IP and a USB driver. The embedded software can be driven directly from the verification environment using Cadence Incisive® Software Extensions, enabling your SoC verification team to begin running sophisticated test scenarios with minimal setup and effort.

The USB PHY is optimized for low power and designed for industry-leading performance, area, and yield. It is available for the most popular process nodes. The entire solution has undergone rigorous testing and meets Cadence quality guidelines for integration-optimized IP.

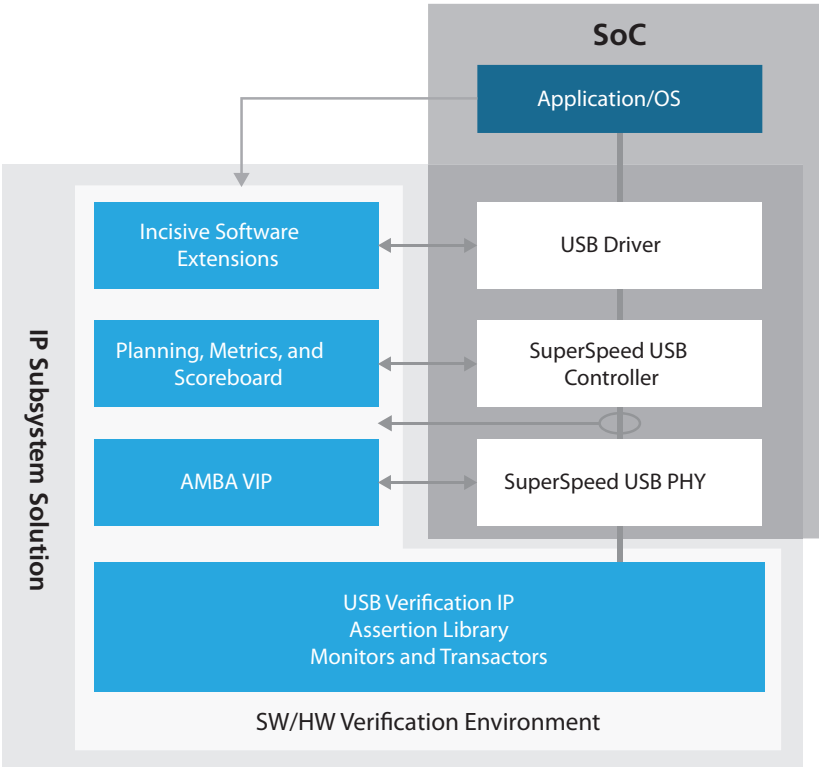

Figure 1: Cadence SuperSpeed USB 3.0 IP Solution

Highlights

- Conforms to the USB 3.0 specification (version 1.0), ECN 1.0, and includes support for the xHCI specification (version 0.97)
- Host controller is highly configurable to ensure optimization for bandwidth, area, and CPU overhead
- Device controller includes optional DMA and configurable resources to ensure effective performance and area tradeoff
- Verification IP is configured to allow easy migration to the SoC-wide verification environment
- Includes a pre-configured USB 3.0 driver as part of the verification environment
- Integration-optimized to reduce the cost, effort, and risk of integration into a larger SoC design

Features

Integration-optimized IP

- Adheres to Cadence guidelines for integration-optimized IP
- Ensures a smooth fit into the SoC development environment
- Comprehensive delivery kit includes support for the Common Power Format (CPF), wreal, and transaction-level modeling (TLM) to streamline integration throughout the development process
- State-of-the-art verification environment is ready to run and easily expandable to the SoC level and beyond
- Configured drivers are integrated with the full HW/SW verification environment
- Packaging and board reference designs are provided

Host controller

- Compliant with USB 3.0 specification version 1.0 and xHCI specification version 0.97

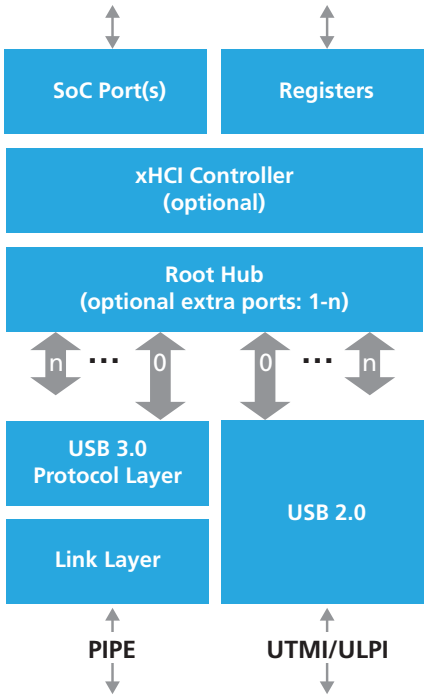

Figure 2: Host controller

- Optional xHCI engine reduces software overhead and includes configurable numbers of device slots and interrupters
- Optional support for host-initiated stream data movement
- Optional root hub with configurable number of ports
- Configurable internal data path width and core frequency (125/250/500MHz) ensures implementation
- USB 3.0 PIPE interface with configurable width (8/16/32 bits)
- Efficient buffering schemes and configurable buffer sizes minimize latency and area
- Low-power support: all USB 3.0 power management modes plus extensive clock tree gating and multiple power wells
- USB 2.0 core with UTMI/ULPI interfaces
- Several SoC bus interfaces available, including AHB, AXI, and a low-latency native interface

Device controller

- Compliant with USB 3.0 specification version 1.0
- Supports control, interrupt, bulk, and isochronous transfers
- Low-power support: all USB 3.0 power management modes plus extensive clock tree gating and multiple power wells
- Configurable internal data path width and core frequency (125/250/500MHz) ensures implementation
- Standard FIFO interface or an optional DMA controller
- Optional endpoint zero block for processing the standard device descriptor
- USB 3.0 PIPE interface with configurable width (8/16/32 bits)
- Several SoC bus interfaces available, including AHB, AXI, and a low-latency native interface
- Configurable number of FIFO sizes, configurations, interfaces, alternative interfaces, and endpoint characteristics
- Optional USB 2.0 core, for backward compatibility, with UTMI/ULPI interfaces

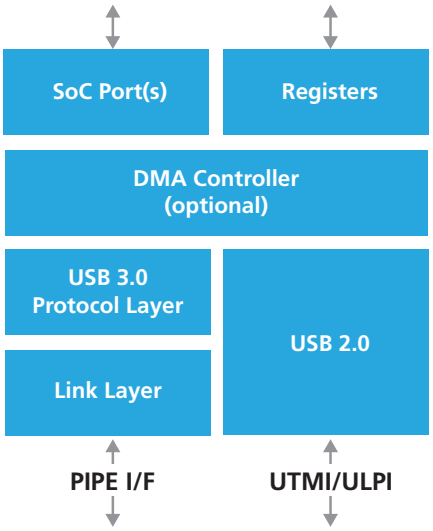

Figure 3: Device controller

PHY

- Compliant with USB 3.0 specification version 1.0
- Spread spectrum clock/data recovery system and data scrambling to minimize EMI
- 8b/10b encode/decode
- Low-power support: all USB 3.0 power management modes plus extensive low-power features
- USB 3.0 PIPE interface with configurable width (8/16/32 bits)
- Advanced mixed-signal analog tools and techniques ensure high yield and margin for package and board variations
- Optional USB 2.0 PHY, for backward compatibility, with UTMI/ULPI interfaces

Verification IP

- Supports protocol versions 1.1, 2.0, OTG, and SuperSpeed USB 3.0
- Integrates with SystemVerilog and e language testbenches
- Conforms with industry-standard Open Verification Methodology (OVM)
- Includes assertion library, bus monitors, and transactors at the transaction level that can be used to create an SoC-wide verification environment
- Includes scoreboards and a Compliance Management System (CMS)

USB Driver

- Fully configured low-level driver enables HW/SW to be verified as a system
- Hardware abstraction layer enables software components to work seamlessly and allows for use in a wide variety of markets and applications
- Portable to multiple operating systems and a wide variety of processor types
- Reference code is provided

Deliverables

- Configurable and synthesizable RTL code
- Easy-to-use test environment, including protocol checkers, bus monitors, and performance monitors
- Configurable synthesis and simulation scripts
- Technical documents, including a Design and Integration Manual
- Cadence tool views

Cadence Services and Support

- Cadence application engineers can answer your technical questions by telephone, email, or Internet—they can also provide technical assistance and custom training
- Cadence certified instructors teach more than 70 courses and bring their real-world experience into the classroom
- More than 25 Internet Learning Series (iLS) online courses allow you the flexibility of training at your own computer via the Internet
- Cadence Online Support gives you 24x7 online access to a knowledgebase of the latest solutions, technical documentation, software downloads, and more

For more details on the Cadence VIP solution, view the following document: http://www.cadence.com/rl/Resources/overview/vip_portfolio_ov.pdf

cadence®

Cadence is transforming the global electronics industry through a vision called EDA360. With an application-driven approach to design, our software, hardware, IP, and services help customers realize silicon, SoCs, and complete systems efficiently and profitably. **www.cadence.com**

21379 11/11 MK/DM/PDF