cadence®

Virtuoso Multi-Mode Simulation

Comprehensive design and verification with the industry's leading simulators

Cadence® Virtuoso® Multi-Mode Simulation combines industry-leading simulation engines to deliver a complete design and verification solution. It meets the changing simulation needs of designers by preserving design intent as they progress through the design cycle—from architectural exploration, to analog and RF block-level development with flexible and reliable abstraction, to final analog and mixed-signal full-chip verification for faster convergence of results.

Virtuoso Multi-Mode Simulation

Virtuoso Multi-Mode Simulation is a comprehensive design and verification solution that combines SPICE, RF, FastSPICE, and mixed-signal simulators in a unique shared licensing package. This unified solution preserves the design intent and delivers scalable performance and capacity through reliable abstraction, providing faster convergence to results for verification of analog, RF, memory, custom digital, and mixed-signal silicon realization.

Virtuoso Multi-Mode Simulation delivers a variety of analyses and measurements in a flexible access model to provide designers with the appropriate simulation technology tailored for each abstraction level of the verification flow.

- Virtuoso Spectre® Circuit Simulator provides a high-precision SPICE simulation of pre- and post-layout analog/RF designs with a comprehensive set of analyses for faster convergence

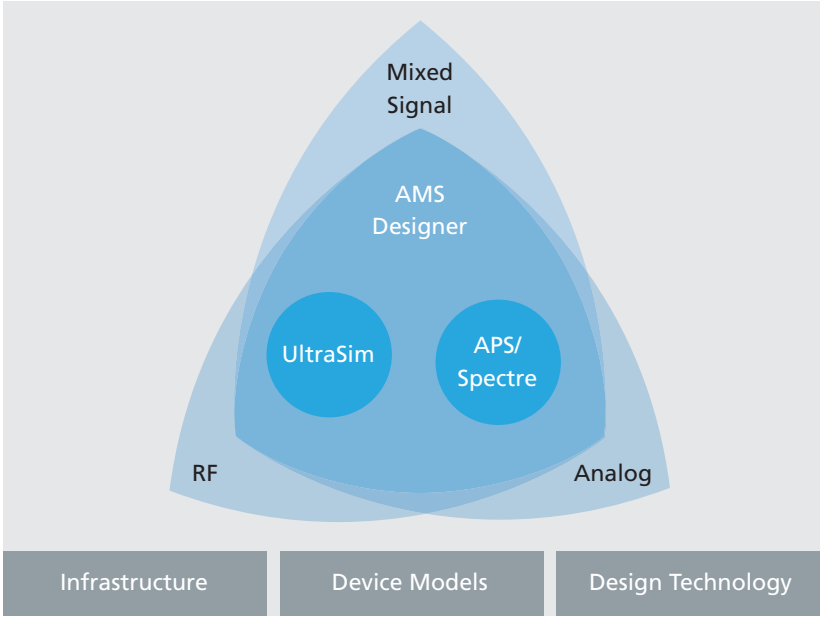

Figure 1: Virtuoso Multi-Mode Simulation offers a complete verification solution for silicon realization

- Virtuoso Accelerated Parallel Simulator delivers high-precision SPICE and scalable multi-core simulation performance for complex and large pre- and post-layout of analog and RF IC designs
- Virtuoso UltraSim Full-Chip Simulator for faster convergence and signoff of post-layout designs at the chip level
- Virtuoso AMS Designer delivers mixed-signal design and verification through reliable abstraction and with a faster convergence

- Virtuoso AMS Designer Verification Option for advanced SoC verification

These simulators support a common syntax, use common device model equations, and are fully integrated into the Virtuoso Analog Design Environment and the Cadence Incisive® design and verification flow. The complementary feature sets of these simulators delivers improved productivity and facilitates adoption as designs move through the architecture, implementation, and verification stages—and as simulation needs change (see Figure 1).

Benefits

Design quality and convergence

- Uses silicon-accurate device models across all simulators that are universally supported by all foundry process design kits (PDKs)
- Supports shared syntax and abstractions across all engines and minimizes translation when moving among design domains
- Features tight integration with the Virtuoso Analog Design Environment—with common use model, cross-probing, and backannotation capabilities
- Features tight integration into the Incisive Logic Design Environment—with common-use model, debugging, waveform viewing, and language support
- Provides a proven, comprehensive suite of high-precision analyses with a simple use model, delivering accurate results
- Offers post-layout simulation and signoff analysis to ensure first-pass silicon realization success

Scalability in performance

- Delivers simulation performance for complex and large analog/RF, custom digital, and mixed-signal designs
- Offers high-performance parallel simulation by harnessing the power of clusters of multi-core compute platforms to deliver peak performance

Productivity

- Provides high-performance and high-capacity transistor-level verification of a wide range of analog, custom-digital, and mixed-signal designs
- Offers flexible and reliable abstraction for analog and digital-centric mixed-signal design flows, delivering faster simulation turnaround time

Features

Silicon-accurate modeling

All Virtuoso Multi-Mode Simulation engines use the same device model equations, eliminating model correlation issues and enabling faster convergence on simulation results. Common equations also ensure that new device model updates are available with all the simulators at the same time.

Greater performance and capacity

Virtuoso Multi-Mode Simulation engines provide the best combination of performance and capacity without sacrificing accuracy.

Language and netlist support

Virtuoso Multi-Mode Simulation supports a variety of abstraction methods. It is compatible with most commonly used SPICE input decks for both pre- and post-layout. It can natively read Spectre, SPICE, and Verilog-A netlist formats and device models. It also supports standard language inputs in Verilog-AMS, VHDL-AMS, Verilog-A, Verilog, and VHDL formats.

Post-layout simulation

Verification for post-layout designs has become increasingly important with advanced nanometer processes. For larger designs such as analog subsystems and full chips, the post-layout parasitics data is growing exponentially at 65nm and below.

Virtuoso Multi-Mode Simulation offers a flexible solution for SPICE-level post-layout simulations of complex and large designs—with tens of thousands of circuit devices dominated by parasitics. Virtuoso Multi-Mode Simulation meets the SoC design verification challenge with a combination of unique hierarchical parasitic stitching techniques and an accurate frequency-based parasitic reduction algorithm. This approach delivers the performance and capacity for post-layout verification of large designs. It also provides an optimized power net simulation technique and methodology for analysis of effects such as IR drop, signal integrity, timing, and substrate degradation.

Design reliability

As gate oxide thickness and dimensions of scale shrink in IC design, reliability problems occur and need to be considered early in the design process. Some of the more problematic issues include negative bias temperature instability (NBTI) and hot carrier injection (HCI). These can lead to problems such as performance degradation, burn-in yield loss, leakage current increase leading to increased power consumption, and even functional failure of ICs.

Virtuoso Multi-Mode Simulation provides a full-chip reliability simulation and analysis solution, enabling designers to consider reliability effects in the early stages of design and ensure silicon realization that has sufficient margins to function correctly over the product's entire lifetime.

Advanced analog and RF circuit analysis techniques

The advanced architecture of Virtuoso Multi-Mode Simulation uses proprietary techniques—including adaptive time step control, sparse matrix solving, and multi-core processing—to provide high performance while maintaining signoff accuracy. It bridges the gap between manufacturability and time to market at advanced process nodes by providing a comprehensive set of statistical analysis tools tailored to IC design. Tight integration with the Virtuoso Analog Design Environment offers user-friendly interactive setup and advanced visualization of statistical results.

Virtuoso Multi-Mode Simulation provides the flexibility to combine design IP from different sources and abstraction levels necessary for the design and verification

of today's advanced mixed-signal SoCs. It accepts designs in combinations of various hardware description languages, allowing analog bottom-up and digital top-down design methodologies to link and enable complete analog/mixed-signal full-chip verification.

Specifications

Comprehensive device models

- MOSFET models, including latest versions of BSIM3, BSIM4; PSP, HISIM, MOS9, MOS11, and EKV
- Silicon-on-insulator (SoI), including latest versions of BTASOI, SSIMSOI BSIMSOI, BSIMSOI PD, and BSIM-IMG
- High-voltage MOSFET models, including latest versions of HVMOS, LDMOS, and HiSim_HV
- TMI models from TSMC
- Bipolar junction transistor (BJT) models, including latest versions of VBIC, HICUM L0, HICUM L2, Mextram, HBT, and Gummel-Poon models
- GaAS MESFET models, includes latest versions of GaAs, TOM2, TOM3, and Angelov
- Rensselaer Polytechnic Institute's (RPI) Poly and Amorphous Silicon Thin-Film models
- Diode, JFET, FinFET, and Flash cell models
- Verilog-A compact device models
- Specialized reliability models (AgeMOS) for hot carrier injection (HTI) and negative bias temperature instability (NBTI) analysis
- Platform support
- x86 32-bit: Redhat Enterprise V5 and V6, SUSE Linux 9 and 10
- x86 64-bit: Redhat Enterprise V4, V5, and V6, SUSE Linux 9 and 10
- Sun Solaris 10

Virtuoso Spectre Circuit Simulator

Virtuoso Spectre Circuit Simulator is an industry-proven, fast, SPICE-accurate simulator for tough analog, radio frequency (RF), and mixed-signal circuit simulation and device characterization. It is tightly integrated with the Virtuoso custom design platform and provides a comprehensive set of detailed transistor-level analyses in multiple domains for faster convergence on design goals. Its superior architecture allows for low memory consumption and high-capacity analysis.

Benefits

- Provides high-performance, high-capacity SPICE-level analog and RF simulation with out-of-the-box tuning for accuracy and faster convergence
- Facilitates the tradeoff between accuracy and performance through user-friendly simulation setup applicable to the most complex analog and custom-digital ICs
- Enables accurate and efficient post-layout simulation with parasitics, S-Parameter models (n-port), and lossy coupled transmission lines (mtline)
- Performs application-specific analysis of RF performance parameters (spectral response, gain compression, inter-modulation distortion, impedance matching, stability, and isolation)
- Offers advanced statistical analysis (Smart, MonteCarlo, and DCmatch) to help design companies improve the manufacturability and yield of ICs at advanced process nodes without sacrificing time to market
- Delivers fast interactive simulation setup, cross-probing, visualization, and post-processing of simulation results through tight integration with Virtuoso Analog Design Environment

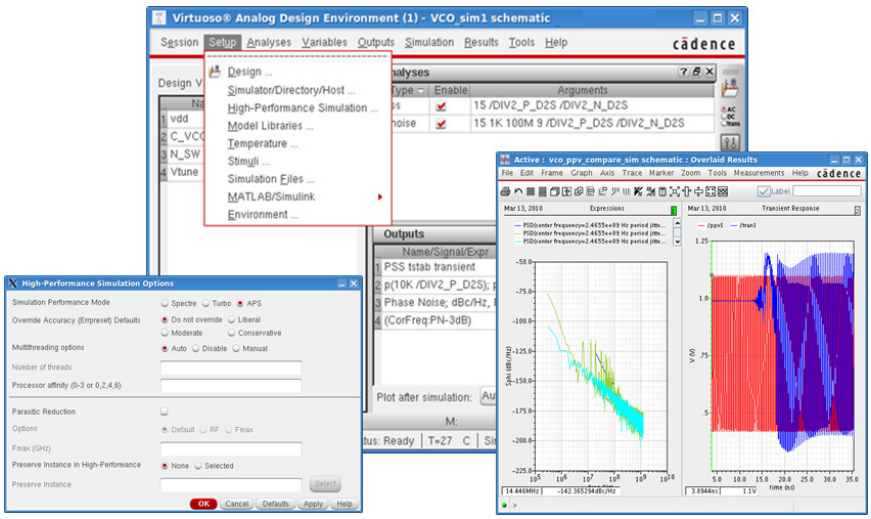

Figure 2: Virtuoso Spectre Circuit Simulator delivers significant performance and capacity for accurate analog simulation for silicon realization

- Ensures higher design quality using silicon-accurate, foundry-certified device models shared across the simulators within the Virtuoso Multi-Mode Simulation solution

Features

Production-proven circuit simulation techniques

Virtuoso Spectre Circuit Simulator uses proprietary techniques—including adaptive time step control, sparse matrix solving, and multi-processing of MOS models—to provide high performance while maintaining signoff accuracy. It includes native support for both Spectre and SPICE syntax, giving users the flexibility to use Spectre technology for any design flow without worrying about the design format. Additionally, it converges to results that are "silicon-accurate" by modeling extensive physical effects in devices for deep sub-micron processes.

Comprehensive statistical analysis

Virtuoso Spectre Circuit Simulator bridges the gap between manufacturability and time to market at advanced process nodes by providing a comprehensive set of statistical analysis tools tailored to IC design. Advanced Monte Carlo algorithms enable smart selection of process and design parameters to characterize the yield in one-tenth of the required simulation runs (see Figure 2). The DC Match capability efficiently analyzes local process mismatch effects and identifies the yield-limiting devices and parameters. Tight integration between Virtuoso Spectre Circuit Simulator and Virtuoso Analog Design Environment offers user-friendly interactive setup and advanced visualization of statistical results.

Transient noise analysis

Virtuoso Spectre Circuit Simulator provides transient noise analysis for accurate calculation of the large signal noise in nonlinear non-periodic circuits. All noise types are supported—including thermal, shot, and flicker. The analysis is built on top of Spectre Circuit Simulator's industry-proven accurate transient engine.

Built-in Verilog-A and MDL

Virtuoso Spectre Circuit Simulator offers design abstraction for faster convergence on results, including behavioral modeling capabilities in full compliance with Verilog-A 2.0. The compiled Verilog-A

implementation is optimized for compact device models offering comparable performance to built-in device models.

In addition to supporting standard SPICE measurement functions (.measure), it offers a measurement description language (MDL) to automate cell and library characterization. Virtuoso Spectre MDL enables the designer to post-process the results and tune the simulator to provide the best performance/accuracy tradeoff for a specific measurement.

Advanced device modeling and support

Virtuoso Spectre Circuit Simulator supports MOS, BJT, specialty transistor models, resistors, capacitors, inductors, transformers and magnetic cores, lossy and lossless transmission lines, independent and controlled voltage and current sources, and Z and S domain sources.

The user-defined model interface includes a compiled model interface (CMI) that is shared across all platform simulators. It allows for the rapid inclusion of user-defined models for a "model once, use everywhere" capability. It offers a curve tracer analysis capability for rapid model development and debugging.

RF simulation

Virtuoso Spectre Circuit Simulator provides a proven and widely adopted set of comprehensive RF analyses capabilities.

- Harmonic balance analysis, optimized for high dynamic range, high-capacity RF circuits with distributed components
- Periodic and quasi-periodic steady-state analysis based on the Cadence patented time-domain shooting Newton algorithm, optimized for strongly non-linear circuits
- Envelope following analysis supporting all analog and digital modulation techniques
- Rapid IP2 and IP3 calculation based on perturbation technology
- Periodic noise analysis for the accurate calculation of noise in non-linear time variant circuits with detailed analysis options (modulated noise, sampled noise, and jitter)
- Noise and distortion summary to identify the contribution of each device to the total output noise, harmonic, or inter-modulation distortion
- Small signal analysis: AC, transfer function, S-Parameters, and stability based on a periodic or quasi-periodic operating point
- Monte Carlo, corner-case, and parametric sweep analysis

Noise-aware PLL analysis

An automated flow for time-domain and jitter analysis of integer-N and fractional-N phase locked loops (PLL) blocks. The flow significantly speeds up PLL verification using abstraction-transistor-calibrated nonlinear models for sub-components of the PLL. The flow enables PLL designers to capture the effect of circuit nonlinearity on closed-loop PLL noise and test for complicated performance parameters such as injection pulling.

RF measurment library

The library consists of RF measurement elements such as noise figure and inter-modulation distortion tailored for specific RF blocks (amplifiers, mixers, and oscillators). Designers can insert the measurements directly on the schematics simplifying simulation setup and post-processing. The measurement element will automatically set up the simulation, perform any necessary post-processing and plot the required waveforms. Users can augment the library by defining their own measurements.

Co-simulation with Simulink

The MathWorks Simulink interface to Virtuoso Spectre Circuit Simulator offers system and circuit designers a unique integrated environment for design and verification. Designers can insert their analog and RF schematics and post-layout netlist directly in the system-level block diagram and run a co-simulation between Simulink and Virtuoso Spectre technologies. Designers can reuse the

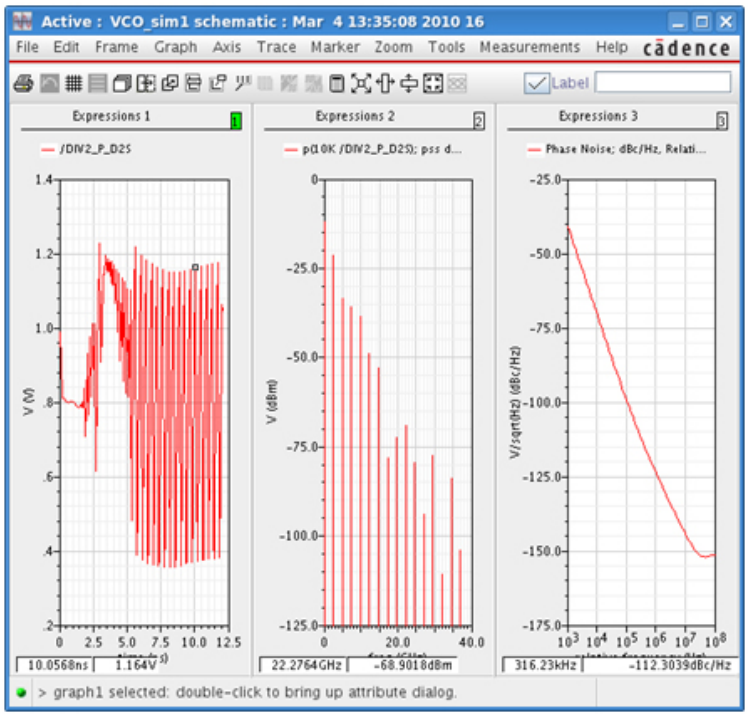

Figure 3: Virtuoso Spectre Simulator offers fast signoff-accurate analysis of voltage-controlled oscillators

same Simulink testbench from system-level design to post-layout verification, minimizing the unnecessary format conversion while maintaining accuracy throughout the design flow.

Virtuoso Multi-Mode Simulation toolbox for MATLAB

The Virtuoso Multi-Mode Simulation toolbox for MATLAB reads PSF and SST2 files directly in MATLAB. Users benefit from the rich set of MATLAB mathematical functions to post-process simulation results from Virtuoso Spectre Circuit Simulator, Virtuoso UltraSim Full-Chip Simulator, and Virtuoso AMS Designer with flexible analog simulation. All sweep types are supported in the toolbox, including Monte Carlo and parametric. Special data structures are used to store RF signals and harmonics resulting from PSS and QPSS analysis. Furthermore, the Virtuoso Multi-Mode Simulation toolbox complements the rich MATLAB libraries with communication product-specific post-processing functions such as Fast Fourier Transform, third-order intercept point, and 1-dB gain compression point.

Post-layout simulation

Virtuoso Spectre Circuit Simulator enables analog and RF block and subsystem post-layout verification at near the speed of pre-layout simulation. An accurate parasitic reduction technique enhances the simulation performance of parasitic-dominant circuits by a significant amount over traditional SPICE-level simulation. The technology enables designers to trade-off accuracy and performance using a simple user-friendly setup.

Specifications

Comprehensive circuit analyses

- DC, AC, and transient analysis
- Noise, transfer function, and sensitivity analysis
- Transient noise analysis
- Native reliability analysis
- Monte Carlo and parametric statistical support
- Full support for sweeping analysis and circuit parameters
- Built-in measurement description language
- Harmonic balance analysis
- Periodic and quasi-periodic steady state analysis (PSS and QPSS) based on shooting Newton technology
- Periodic and quasi-periodic noise analysis
- Periodic and quasi-periodic small signal analysis
- Periodic stability analysis
- Time-domain and frequency-domain envelope analysis
- Perturbation-based rapid IP2 and IP3
- Noise and distortion summaries
- Co-simulation with Simulink from The MathWorks
- Virtuoso Multi-Mode Simulation toolbox for MATLAB from the MathWorks

Design inputs/outputs

- Virtuoso Spectre netlist format
- SPICE netlist format
- Verilog-A 2.0
- S-Parameter data files
- PSF waveform format

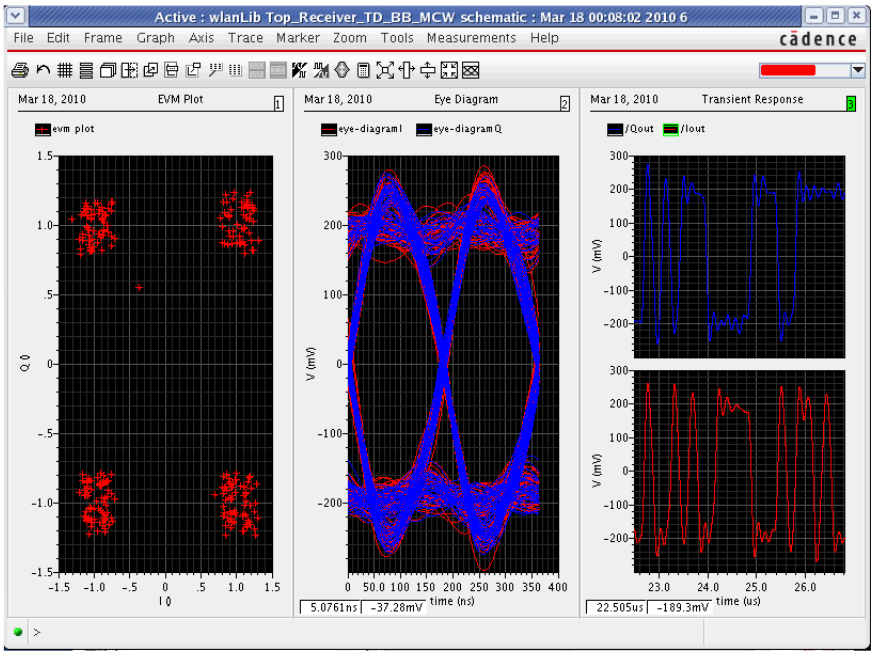

Figure 4: Virtuoso Multi-Mode Simulation RF analysis enables fast transceiver verification

Virtuoso Accelerated Parallel Simulator

Virtuoso Accelerated Parallel Simulator, a key component of the Virtuoso Multi-Mode Simulation, provides advanced performance for the next generation of analog and RF simulation. It delivers significant scalable performance and capacity at full Spectre accuracy across a broad range of complex analog, RF and mixed-signal blocks, and sub-systems with sizes up to millions of transistors and passive and parasitic elements. Virtuoso Accelerated Parallel Simulator provides all the transistor-level analysis capabilities available in Virtuoso Spectre Circuit Simulator. Additionally, its proprietary parallel simulation technology delivers scalable multi-core processing capability on modern multi-core compute platforms.

Benefits

- Provides significant single-core performance with an identical use model and full Spectre accuracy for everyday simulation of complex and/or large block designs, leading to faster convergence
- Enables high-precision simulation for large post-layout analog and RF designs and subsystems dominated by parasitic devices
- Delivers scalable performance leveraging a single machine or cluster of machines with multi-core architectures, allowing higher levels of analog design integration and verification and a quick turnaround time on simulation
- Enables fast and accurate analysis of complete transceivers and large post-layout RF IC blocks by significantly improving the performance and capacity of harmonic balance analysis using a multi-core compute platform

Features

- Supports all analyses capabilities offered in the Virtuoso Spectre Circuit Simulator
- Offers advanced parallel simulation on a single multi-core compute platform
- Supports distributed, advanced parallel simulation across a cluster of multi-core compute platforms
- Enables parasitic stitching and reduction for post-layout design and verification, providing additional performance gain for analog and RF designs dominated by parasitics
- Multi-core harmonic balance and envelope analysis
- Full support of RF components and measurements library with identical-use model to standard RF simulation capabilities in the Virtuoso Spectre environment

Specifications

Comprehensive device models

- MOSFET models, including latest versions of BSIM3, BSIM4; PSP, HISIM, high-voltage MOS (HVMOS), MOS9, MOS11, and EKV
- Silicon-on-insulator (SOI), including latest versions of BTASOI, SSIMSOI BSIMSOI, BSIMSOI PD, and BSIM-IMG
- Bipolar junction transistor (BJT) models, including latest versions of VBIC, HICUM, Mextram, HBT, and Gummel-Poon models
- Diode, JFET
- GaAS MESFET models, includes latest versions of GaAs, TOM2, TOM3, and Angelov
- Rensselaer Polytechnic Institute's (RPI) Poly and Amorphous Silicon Thin-Film models
- Verilog-A compact device models
- Specialized reliability models (AgeMOS) for hot carrier injection (HTI) and negative bias temperature instability

Circuit analysis

- DC, AC, and transient analysis
- Transient noise analysis
- Native reliability analysis
- Monte Carlo and parametric statistical support
- Full support for sweeping analysis and circuit parameters
- Built-in measurement description language
- RF harmonic balance analysis
- RF shooting Newton analysis
- RF FAST envelope analysis supporting all modulation schemes
- RF noise and small signal analysis based on harmonic balance solution

Design inputs/outputs

- Virtuoso Spectre netlist format
- SPICE netlist format
- Verilog-A
- S-Parameter data files
- PSF waveform format

Virtuoso UltraSim Full-Chip Simulator

Virtuoso UltraSim Full-Chip Simulator

The Virtuoso UltraSim Full-Chip Simulator is a high-performance transistor-level FastSPICE circuit simulator for pre- and post-layout verification of memories, custom-digital, and analog/mixed-signal SoC designs. It delivers the capacity, accuracy, and speed required for verification using abstraction where appropriate while preserving the design intent. It uses true hierarchical simulation and a patented isomorphic and adaptive partitioning algorithms

Benefits

- Accelerates pre-and post-layout simulation for a wide range of applications from blocks to full-chip SoCs (see Figure 5)
- Provides a comprehensive set of transistor-level analysis covering electrical rule check (ERC), power, timing, and nodal activity (see Figure 6)
- Handles large post-layout designs using a combination of unique hierarchical parasitic stitching techniques and an accurate frequency-based parasitic reduction algorithm
- Supports multiple simulation abstraction modes (SPICE, analog, mixed-signal, and digital), enabling the user to locally tune performance and accuracy settings for different blocks in the design
- Flexible easy-to-use controls for providing adequate tradeoff between accuracy and simulation speed
- Plugs smoothly into design and verification flows through integration with Virtuoso Analog Design Environment and command-line environments

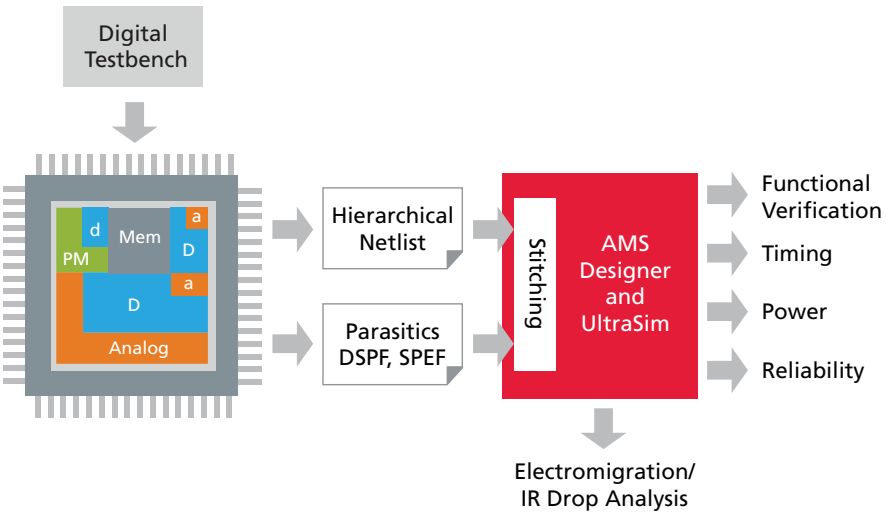

Figure 5: Virtuoso UltraSim post-layout verification and analysis for silicon realization

Features

Compatible with SPICE, Spectre, Verilog-A, and SPEF

Virtuoso UltraSim Full-Chip Simulator is compatible with most types of SPICE input decks for both pre- and post-layout. Natively reads Virtuoso Spectre format netlists and models, and uses the same views within Virtuoso Analog Design Environment, making it easy to adopt in Virtuoso Spectre-based design flows.

Post-layout simulation

When used in conjunction with Cadence post-layout products, Virtuoso UltraSim Full-Chip Simulator provides a means for exploration and validation of such effects as electromigration, IR drop, signal integrity, and substrate degradation. It also has built-in, state-of-the-art, S-Parameter–based parasitic reduction for faster simulation with minimal loss in accuracy.

Electrical Rule Check	Power Analysis	Timing Analysis	Node Activity Analysis
MOSFETs connected across different power domains	Average, RMS, peak-to-peak power and total energy at the chip and block level	Excessive rise and fall times	Glitch check
Floating gates, floating bulks, and dangling nodes	Current hot spots	Setup, hold, pulse width and timing edge errors	Overshoot, undershoot, toggling, and note capacitance
MOSFET shorting VDD and GND	Wasted capacitive currents		Signal probablility of being high or low
Always conducting MOSFET	Floating gate-induced leakage	User-defined measurements using SPICE measure	
NMOS-VDD, PMOS-GND connections			Static: device parameters, voltage checks, and high-impedance nodes
Forward-biased substrate	Static: DC leakage path		

Figure 6: Virtuoso UltraSim transistor-level full-chip analysis for silicon realization

Design reliability simulation

Virtuoso UltraSim Full-Chip Simulator provides a robust set of analyses capable of predicting and validating timing, power, and reliability. It is the only FastSPICE simulator capable of simulating hot carrier injection (HCI) and negative bias temperature instability (NBTI)—key stress effects that must be taken into account for high-performance advanced node designs.

Specifications

Design inputs and outputs

- Virtuoso Spectre netlist
- SPICE netlist format
- DSPF/SPEF parasitic formats
- Verilog-A
- SST2 waveform format
- PSF and PSF XL waveform format
- FSDB format
- Veritools waveform format
- Virtuoso UltraSim/Verilog
  - Verilog-HDL IEEE 1364
  - PLI 1.0, VPI (PLI 2.0)
  - SDF
- AMS-Virtuoso UltraSim
  - Verilog-AMS 2.0
  - VHDL-AMS 1076.1
  - Verilog (IEEE 1364-1995, IEEE 1364-2001 extensions)
  - VHDL (IEEE 1076-1987, IEEE 1076-1993, IEEE 1076.4-2000 [VITAL 2000])
  - PLI 1.0, VPI (PLI 2.0)
  - SDF
  - SystemC™, SystemVerilog

Virtuoso AMS Designer Simulator

Virtuoso AMS Designer provides an advanced mixed-signal simulation solution for the design and verification of analog, RF, memory, and mixed-signal silicon realization. It is integrated with the Virtuoso full-custom environment as well as the Incisive functional verification platform. Virtuoso AMS Designer provides a single simulation executable with flexible abstraction support through the standard mixed-signal languages (Verilog-AMS and VHDL-AMS) and/or SPICE-level models. As the bridge between analog and digital domain, it enables users to choose the right analog solver for the right design or verification task. Designers can choose Spectre technology for SPICE-accurate block-level analog and RF designs, Virtuoso Accelerated Parallel Simulator for SPICE-accurate, scalable high performance, or Virtuoso UltraSim Full-Chip Simulator for silicon realization.

Virtuoso AMS Designer is fully configurable across the design and verification domains, offering the right simulation technology and environment for every stage in the design and verification cycle.

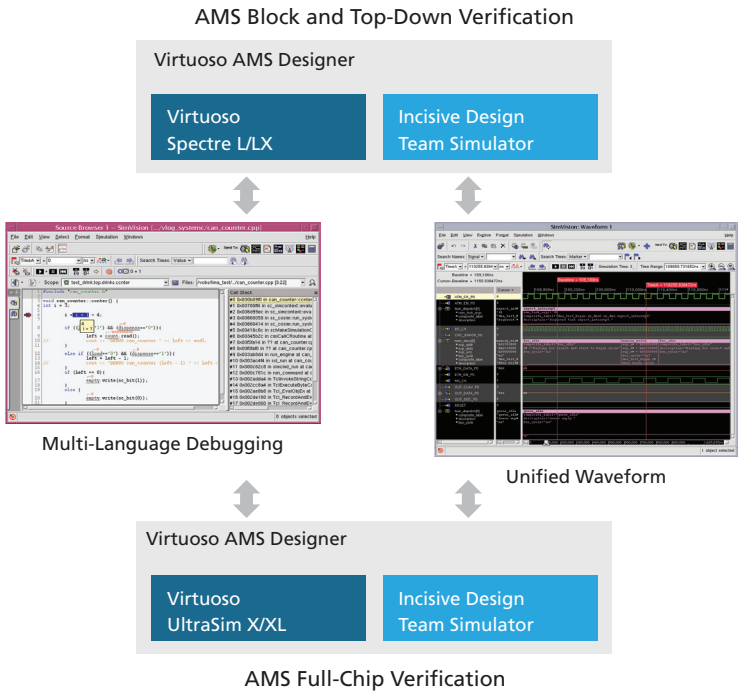

Figure 7: Virtuoso AMS Designer verification flow addresses silicon-realization requirements throughout the design cycle

Benefits

- Ensures design quality with proven Virtuoso analog and Incisive digital simulation technologies
- Supports both analog design flow use models in Virtuoso Analog Design Environment as well as digital verification use models in the Incisive environment
- Supports both top-down and bottom-up methodologies to quickly detect and fix design failures early in the design cycle, helping to meet tapeout schedules
- Extensive language support allows higher level of abstraction and accelerates simulation to achieve faster turnaround time
- Supports simulation of RF circuits at full SPICE accuracy by combining envelope analysis of RF transceivers with digital baseband simulation for faster convergence of results

Features

Methodology-independent design convergence

Virtuoso AMS Designer provides the flexibility to combine IP from different sources and in different formats for today's SoC designs. It does more than just co-simulate analog and digital blocks. By treating Virtuoso Schematic Editor blocks and textual descriptions equally, Virtuoso AMS Designer allows different points of data entry. It accepts descriptions in the standard language formats of Verilog-AMS, VHDL-AMS, Verilog-A, Verilog, VHDL, and SystemC, as well as SPICE and Virtuoso Spectre simulation, or any combination of these languages. This allows bottom-up and top-down design methodologies to converge into a fully functional design.

Different levels of abstraction, such as Verilog-AMS or VHDL-AMS behavioral models and schematic representation, are easily interchangeable to allow the design to change over time from full behavioral to full transistor. The entire design is configured using the hierarchy editor, which facilitates the viewing and design preparation of a complex mixed-signal design. Automatically inserted interface elements are used to translate signals from one domain to the next, leaving the user free to simulate with different design configurations to easily tradeoff simulation speed for simulation accuracy.

Virtuoso AMS Designer also supports IP encryption using RSA technology, which allows the user to establish both IP reuse and virtual-prototyping methodologies.

Integrated with proven Virtuoso and Incisive simulation technologies

Virtuoso AMS Designer is a single executable mixed-signal simulator based on the proven technology of Virtuoso Spectre, Virtuoso Accelerated Parallel

Simulator, UltraSim Full-Chip Simulator, and the Incisive digital simulation capabilities.

Analog-centric flow with Virtuoso

Virtuoso AMS Designer is tightly integrated with the Virtuoso Analog Design Environment for mixed-signal block design. It uses native Analog Design Environment netlisting technologies to combine schematics and behavioral views, enabling users to independently manage the level of abstraction of each block. The entire design is configured using the hierarchy editor, which facilitates the viewing and design preparation of a complex mixed-signal design.

- Using Virtuoso AMS Designer with Virtuoso Spectre Simulatoror, Virtuoso Accelerated Parallel Simulator ensures that the user gets golden simulation results for performance measurements
- Advanced circuit analysis such as Monte Carlo can be performed with the AMS/Spectre interface, leveraging the performance benefits of behavioral models and using the same setup as the Spectre tool
- Advanced-model validation capabilities allow users to verify their circuit design against a behavioral model automatically by comparing simulation waveforms

Digital-centric flow with Incisive

Virtuoso AMS Designer works natively in the Incisive environment for digital-centric verification. A single control file is used to define how analog blocks are integrated into the digital SoC. Analog and RTL blocks can be easily interchanged to trade off accuracy and performance. It supports all features in the Incisive environment like testbench analysis, Specman® technology, and verification planning.

- Automatically inserted interface elements are used to translate signals from one domain to the next, leaving the user free to simulate with different design configurations to easily trade off simulation speed for simulation accuracy
- In the verification flow, the Virtuoso UltraSim Full-Chip Simulator is used as the built-in analog simulation engine. This enables final verification of the largest mixed-signal SoCs. The Incisive digital simulation engine inside Virtuoso AMS Designer delivers high-performance native Verilog, SystemVerilog, VHDL, and SystemC and *e* simulation
- The SimVision multi-language debugging environment allows users to view analog and digital signals in a single waveform environment

Virtuoso AMS Designer Verification Option

Virtuoso AMS Designer Verification Option provides a complete solution for advanced mixed-signal silicon realization.

- Enables cross-domain connectivity between testbenches and design IP blocks from multiple vendors by providing native connectivity between VHDL or SystemVerilog and SPICE
- Supports assertion-based verification for analog and digital designs by extending the syntax of PSL and SVA languages, providing an efficient and effective methodology for capturing design intent and verification automation
- Extends mature digital verification methodologies, such as low-power verification, to the analog domain. Supports capturing power intent with CPF and automatically inserting "PowerSmart" connect modules on key interfaces

Specifications

Virtuoso environment

- Direct Verilog-AMS netlisting
- Hierarchy editor AMS plug-in
- Hierarchy editor configuration
- Support for global design variables and global signals
- Inherited connections

Virtuoso AMS Simulator

- Single executable mixed-signal/mixed-language simulator
- Built-in Virtuoso Spectre, Virtuoso Accelerated Parallel Simulator, or Virtuoso UltraSim simulators and Incisive digital engines
- Digital and Real number-modeling capabilities
- System-level simulations with links to Simulink from the MATHWORKS
- Save/restart
- Common mixed-signal waveform database

Incisive environment

- Mixed-signal debugger
- Breakpoints on time, position, and condition
- Debug stepping through behavioral code, analog, and digital
- Schematic tracer
- Signal flow and error browser
- Digital transaction support

Virtuoso AMS Designer Verification Option

- Native VHDL-SPICE connectivity
- Native SystemVerilog to SPICE and AMS connectivity
- PowerSmart connect modules for low-power support

Design inputs

- Cadence CDBA database or OpenAccess database
- Verilog-AMS 2.0
- VHDL-AMS 1076.1
- Verilog (IEEE 1364-1995, IEEE 1364-2001 extensions)
- VHDL (IEEE 1076-1987, IEEE 1076-1993, IEEE 1076.4-2000 [VITAL 2000])
- Spectre and SPICE netlist formats
- SystemVerilog (IEEE-1800)
- Common Power Format (CPF)

- Within Incisive platform: SystemC (OSCI SystemC v2.01), SystemC Verification Library (OSCI SCV 1.0), and Specman *e*

Design outputs

- SST2 waveform format analog and digital data
- PSF waveform format for analog data
- Verilog-AMS netlist format

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