VIRTUOSO LAYOUT SUITE FAMILY

The Cadence® Virtuoso® Layout Suite family of products delivers a complete solution for front-to-back custom analog, digital, RF, and mixed-signal design. It preserves design intent throughout the entire physical implementation process while managing multiple levels of design abstractions at device, cell, block, and chip levels. Part of the industry-standard Virtuoso custom design platform, Virtuoso Layout Suite optimizes and accelerates layout implementation, and it provides the fastest path to convergence on design goals for realizing mature and advanced node silicon.

VIRTUOSO LAYOUT SUITE FAMILY

The Virtuoso Layout Suite family of products comprises the layout environment of the industry-standard Virtuoso custom design platform, a complete solution for front-to-back custom analog, digital, RF, and mixed-signal design. The Virtuoso Layout Suite preserves design intent throughout the entire physical implementation process, while managing multiple levels of design abstractions from device, cell, and block levels through to the full-chip level. It provides the fastest path to design convergence for mature and advanced node silicon realization.

The Virtuoso Layout Suite includes three tiers of increasing layout automation and designer productivity. By selectively automating aspects of custom-analog design and providing advanced technologies integrated on a common
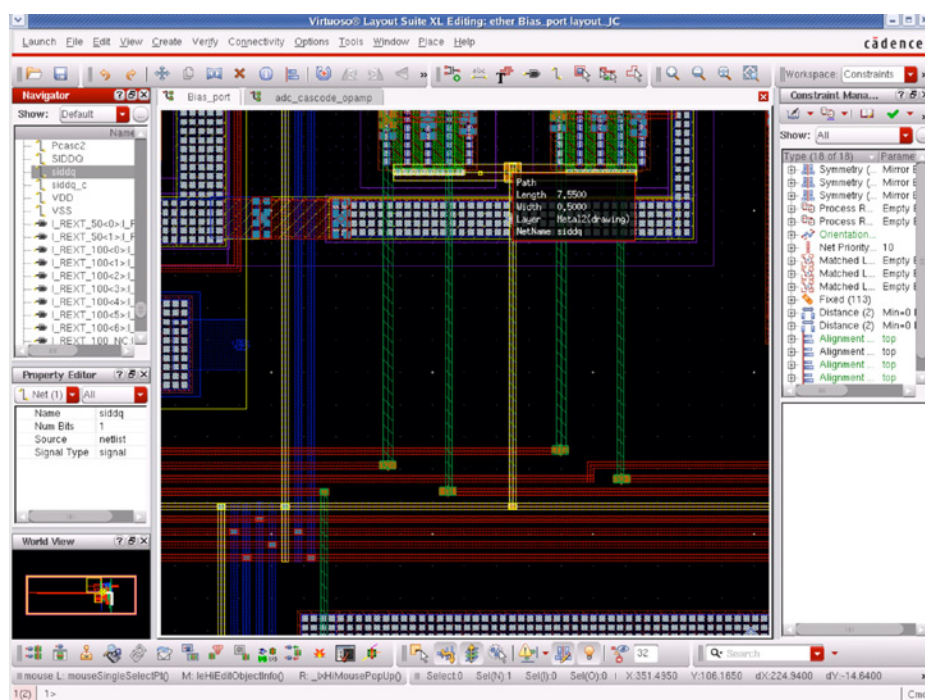

Figure 1: The industry-standard Virtuoso Layout Suite user interface

cādence

database, engineers can focus on precision-crafting their designs without sacrificing creativity to repetitive manual tasks. The suite consists of:

- Virtuoso Layout Suite L, a basic design-creation and implementation environment focused on layout productivity
- Virtuoso Layout Suite XL, an extension to the L tier, is built upon common design intent—the connectivity- and constraint-driven environment at the core of the Virtuoso platform
- Virtuoso Layout Suite GXL, an extension to the XL tier, adds a robust set of advanced automated finishing tools to satisfy demanding physical design tasks such as floorplanning, placement, routing, and optimization; these technologies are the fundamental building blocks to rapidly realizing first-time successful silicon

VIRTUOSO CUSTOM DESIGN PLATFORM

The Virtuoso custom design platform integrates Virtuoso Schematic Editor, Virtuoso Analog Design Environment, Virtuoso Multi-Mode Simulation, and the Virtuoso Layout Suite to speed convergence on design goals at every step for front-to-back custom analog, digital, RF, and mixed-signal design flows. The platform is backed by the largest number of process design kits (PDKs) available from the world's leading foundries, for process nodes everywhere from mature 0.35um to advanced 28nm. It is built on the OpenAccess database, engineered by Cadence for industry-wide interoperability.

The Virtuoso custom design platform also interoperates with the Cadence Encounter® digital implementation platform technologies via the OpenAccess database, providing a single, complete, coherent, and unified representation of design intent. This design intent is preserved throughout the entire physical implementation phase while operating with multiple levels of design abstractions (device, cell, block, chip), speeding design convergence to realize silicon for complex mixed-signal and system-on-chip designs.

BENEFITS

- Supports a variety of design flows and needs with a tiered set of tools
- Eases creation and navigation of complex designs
  - Modern, redesigned common user interface
  - Docked assistants around the layout canvas
- Boosts layout productivity with easy-to-use, easily accessed editing functions
  - Unlimited hierarchical support
  - Multi-window, multi-tabbed environment
  - Rich set of assisted wire-editing functionalities
- Addresses next-generation design problems with common design intent using a connectivity- and constraint-driven environment
  - Generates a correct-by-construction layout through constraint-aware and design-rule–driven editing
  - Automatically ensures real-time process-design–rule correctness
  - Captures and drives common hierarchical design intent with Virtuoso Schematic Editor
  - Supports full-custom analog and custom-digital placement that is fully design-intent and design-rule aware
- Uses SKILL Pcells to optimize design layout and boost productivity
  - Automates editing such as abutment, pin permutation, folding, chaining, and cloning
  - Express SKILL Pcells dramatically improve performance and third-party interoperability
  - Offers advanced module generation for complex interdigitation patterns

- Built on the OpenAccess database
  - Reduces risk of re-spins with a unified representation of design intent across custom and digital implementation
  - Efficiently handles large, high-performance designs
- Offers menu-driven or programmable multi-part path features for guard rings, slotting, etc.
- Offers advanced cloning capabilities for generating and editing complex repeated layout patterns
- Enables more complex levels of design integration with automatic and dynamic design abstraction
- Offers fully automated process retargeting via hierarchical layout migration
- Speeds convergence on advanced node design goals
  - Supports high-performance, high-capacity space-based routing
  - Supports region-based, interactive design-rule-check fixing
  - Optimizes yield based on design intent and recommended design rules

FEATURES

HIERARCHICAL, MULTI-WINDOW, MULTI-TABBED EDITING ENVIRONMENT

Virtuoso Layout Suite enables users to open multiple cells or blocks in a single editing session, or to open different views of the same design, ensuring consistency in complex designs. Users can also open and manage their designs more quickly by using tabs, bookmarks, and history—similar to the functionality in today's popular web browsers.

A tabbed approach to viewing layouts simplifies window management and provides fast access to multiple designs in an intuitive manner. This is particularly helpful when copying portions of a layout from one design to another, or when using a pre-existing design as a reference.

Users can bookmark commonly accessed designs or view the history of opened designs. Bookmarks can be a single cell or a group of cells that appear in individual tabs. A "personal bookmarks toolbar" makes accessing commonly used bookmarks extremely quick and easy.

Virtuoso Layout Suite GXL shares the same look and feel with Virtuoso Schematic Editor and Virtuoso Analog Design Environment. This consistent use model enables a fully featured, intuitive, front-to-back design flow.

DOCKED LAYOUT ASSISTANTS

Docked assistants are user-interface widgets that surround the main layout editing canvas. Virtuoso Layout Suite includes a rich set of assistants, including

Figure 2: Docked layout assistants include a Design Navigator, Property Editor, and World View, which enhance layout productivity

a Design Navigator and Property Editor, Search, and World View Assistants that significantly increase layout productivity.

Through the Design Navigator, users can quickly access specific cells that may be in a lower level of the design hierarchy via a tree browser built into the Design Navigator. Cells, nets, and pins can also be selected, sorted, and probed through the Design Navigator. This is a very effective feature when designing and debugging complex layouts.

The Property Editor Assistant is a new twist on the traditional "Edit Properties" pop-up form. The streamlined interface improves the effective area of the layout canvas space while decreasing mouse clicks and wasteful pop-up dialog boxes.

Through the Search Assistant, layout engineers have comprehensive search capabilities. The Search Assistant categorizes the "found" items into logical groups (cells, pin names, properties, etc.) and displays these items in a tree structure. This makes it very easy for users to find and access information within the design, the design libraries, menu commands, and even the SKILL manuals. Context-sensitive menus and double-click operations allow for rapid operations on selected results.

The World View Assistant is an intuitive navigational aid that allows users to always see the entire design, even while zoomed into a specific section of the layout. This Assistant is particularly useful when working with large layouts where users have to perform editing while zoomed in on a portion of the design. The ability to concentrate on a specific section of layout while still viewing the overall layout decreases the need for repetitive panning and zooming. This translates into fewer mouse clicks, which improves layout productivity.

FLEXIBLE SKILL PCELLS

SKILL parameterized cells (Pcells) provide an advanced level of design automation to minimize tedious and repetitive layout tasks. Pcells support the changing of the size, shape, or contents of each cell

instance without changing the original cell. They raise the level of abstraction to the component level, simplifying complex shapes and devices that can be generated, edited, and managed with variable settings. This results in faster design entry, accelerated layout, and fewer design-rule violations.

HIGHLY CUSTOMIZABLE EDITING FEATURES

The architecture and implementation of the Cadence Design Framework II and the OpenAccess database allow Virtuoso Layout Suite to offer a customizable layout-editing environment and user-added features. This is made possible through the support of the flexible, powerful, and industry-proven SKILL programming language, which gives users direct access to the design database and tools to meet the design requirements of any custom design methodology. Additionally, the OpenAccess database supports a C-based API and toolbox to allow for tool customization and tool interoperability.

DESIGN-RULE–DRIVEN EDITING

Virtuoso Layout Suite provides real-time design-rule–driven editing that flags violations and automatically enforces design rules while the layout is being created. This promotes correct-by-construction layout, improving productivity and eliminating physical verification iterations. All technology file process rules are supported, including complex sub-32nm nodes.

ADVANCED LAYOUT AUTOMATION

Virtuoso Layout Suite simplifies and optimizes block authoring with advanced layout automation features that leverage the design-rule–driven functions and flow. Dynamic Measurement minimizes the need to manually measure geometries. Alignment speeds up the task of aligning instances, pins, and objects. Mark Net efficiently traverses the physical design hierarchy and performs continuity checking and highlighting.
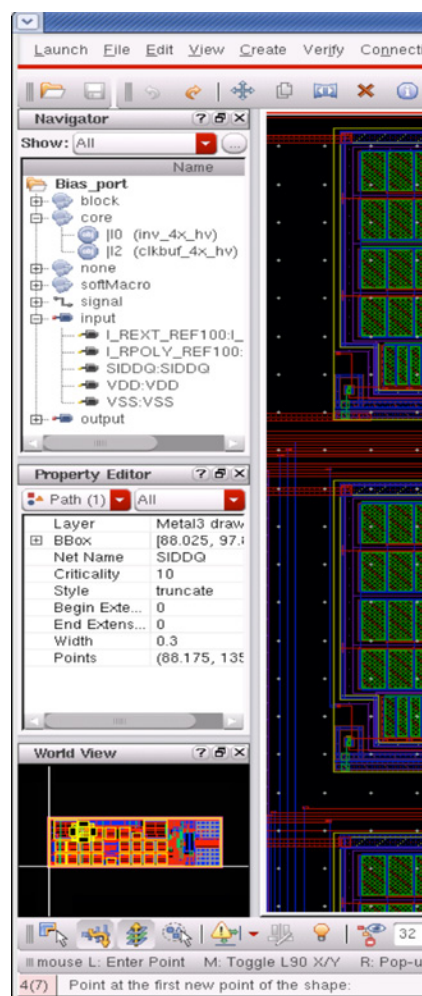
CONNECTIVITY-DRIVEN FUNCTIONS AND FLOW

Virtuoso Layout Suite changes the way custom block authoring is done. Driven by schematic connectivity and constraint design intent established in Virtuoso Schematic Editor or a netlist source (such as CDL or SPICE), an LVS-correct layout can be done in real-time. This ensures correct-by-construction layout, higher productivity, and shorter verification time. Additionally, tedious design tasks can be automated, such as device generation, placement, and routing. Schematics and layout can be cross-probed to highlight instances and devices as well as quickly identify unconnected nets.

In Virtuoso Layout Suite, a new incremental connectivity-driven binding technology has been introduced. This approach is far superior to traditional name-based schematic-to-layout binders, which had severe limitations when supporting schematic-to-layout name mismatches. The connectivity-driven binder enables better support of legacy layouts that have name mismatches, and also improves handling of engineering charge orders (ECOs) that involve renaming of instances and terminals in the layout. The incremental nature of the connectivity binder also greatly improves the performance of a connectivity-driven layout flow.

CONSTRAINT- AND DESIGN-RULE–DRIVEN FUNCTIONS

The Virtuoso platform is built upon a common constraint environment to ensure correct-by-construction layout, higher productivity, and fewer physical verification iterations. Topological constraints, electrical constraints, and/or design-rule specific constraints complete the design intent specified and managed in Virtuoso Schematic Editor, Virtuoso Analog Design Environment, or Virtuoso Layout Suite. Simply set the design intent constraints in Schematic Editor and Layout Suite can easily be configured to either enforce the constraints while generating
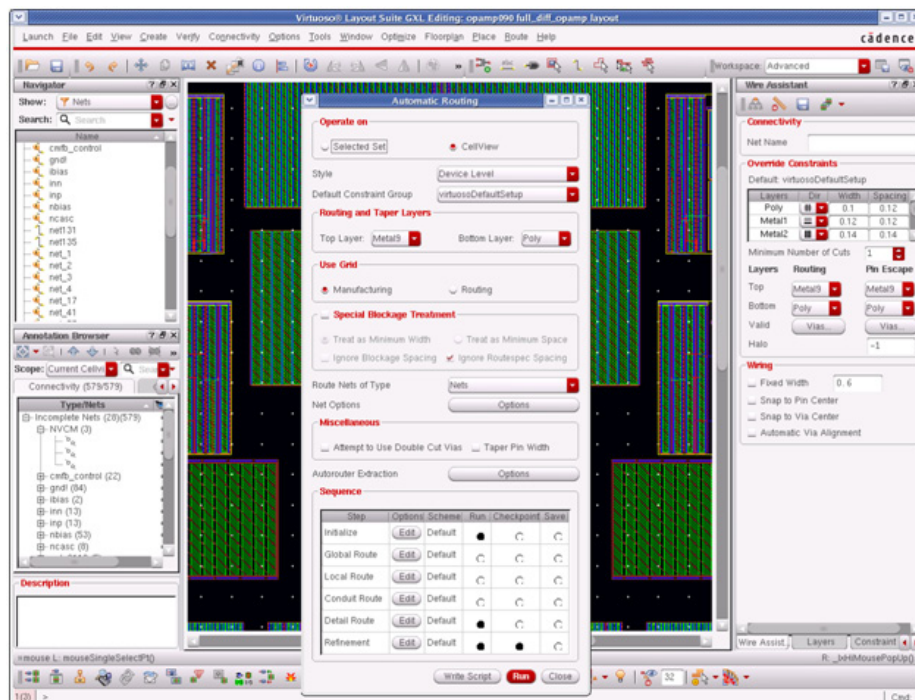

Figure 3: The GXL configuration is integrated with Virtuoso Space-Based Router, a hierarchical, gridless, space-based, full-chip, block- and device-level routing system

layout or automatically flag and log constraint violations that can be discussed at subsequent design reviews.

Integrated signoff constraint verification can be run and accessed from the docked annotation browser, simplifying the task of verifying that a design is meeting the design intent specification. Constraint verification can be done before, during, or after physical implementation of a design.

ADVANCED ASSISTED WIRE EDITING

Virtuoso Layout Suite has a robust set of constraint/design-rule–driven assisted wire-editing capabilities. This comprehensive, fully interactive wire editor is natively integrated into Virtuoso Layout Suite GXL and supports advanced process nodes along with an array of custom specialty routing types such as bus/bundle, differential pair, matched length, and symmetric.

In addition to driving the wire editor fully manually, users can also take advantage of the wire editor's assisted capabilities. Commands such as point-to-point, finish wire, pushing and shoving

of wires, along with guided routing on single nets and buses, are built upon the Virtuoso common constraint system and connectivity-driven layout. These features are productivity enablers for almost all layout engineers, who no longer need to generate complicated scripts to get desired results.

ADVANCED EDITING WITH CLONING

Virtuoso Layout Suite has a unique capability that allows users to "clone" portions of the layout without altering connectivity. What differentiates cloning from a more traditional copy of geometry is that cloning supports both a geometric copy and a connectivity update. This capability is essential in today's connectivity-driven methodologies. In addition to cloning, synchronous clones enable a single change in a member of a clone to update all partner clones. This capability greatly boosts productivity when working in a connectivity-driven environment.
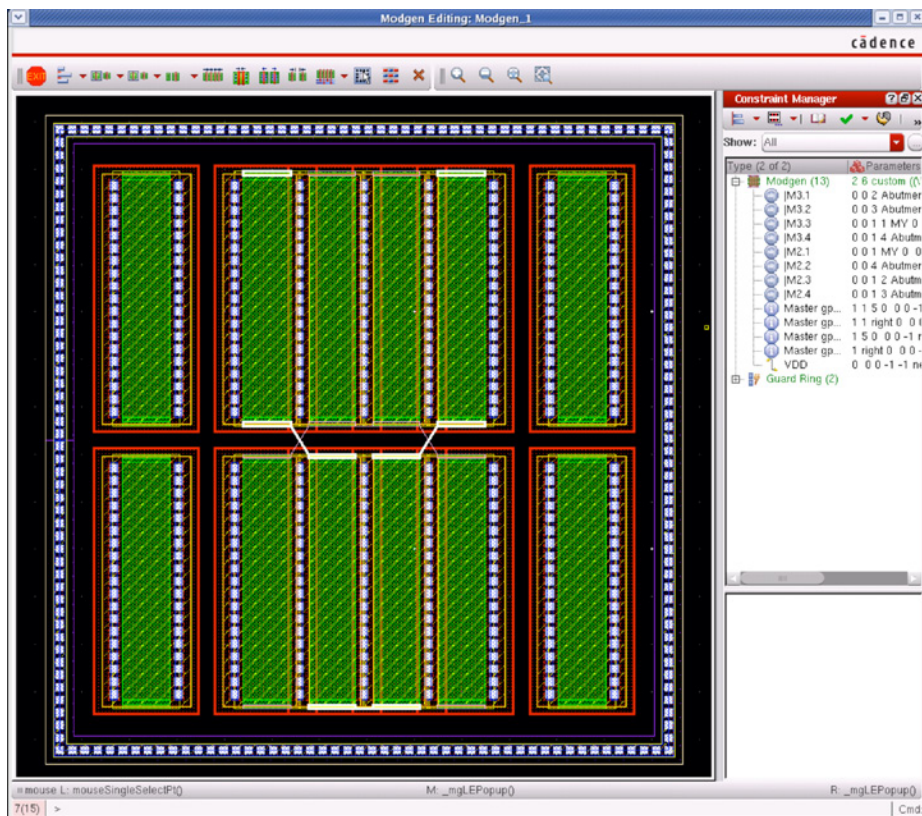
Figure 4: Virtuoso module generators easily generate complex interdigitation schemes and are ideal for highly matched structures such as differential pairs, current mirrors, and other commonly arrayed devices

FULL-CUSTOM FLOORPLANNING

The Virtuoso floorplanner contains automatic and interactive floorplanning tools and technologies that help mixed-signal designers develop layout from a schematic in a methodical manner. The floorplanner supports I/O constraints files, soft and hard rectilinear blocks, layout and abstract views, and digital/custom block types. It has common floorplanning capabilities such as congestion analysis, pin optimization, the ability to generate physical hierarchy, and the ability to configure the layout hierarchy in an efficient graphical manner. The floorplanner is unique in its ability to add value in both top-down and bottom-up methodologies.

ADVANCED MODULE GENERATION

Module generators (MODGENs) are designed to provide layout designers an intuitive way to quickly generate SKILL Pcell instances into a complex, highly matched, and structured array. Within the MODGEN tool, users specify the devices to be arrayed, then specify an interdigitation pattern, and then they

VIRTUOSO SPACE-BASED ROUTER

Virtuoso Space-Based Router is a hierarchical, gridless, space-based, full-chip, block- and device-level routing system for advanced analog, mixed-signal, and custom-digital designs. It has been used for production routing on design using processes from 0.5um to 28nm. The routing environment is native to Virtuoso Layout Suite GXL configuration and is tightly coupled with the Virtuoso common constraint environment. It is a multi-threaded routing environment, capable of routing multimillion-net designs.

Virtuoso Space-Based Router also supports a robust set of specialty custom routing types such as bus/bundle, differential pair, pin-to-trunk, and shielded. These common types of custom routing can be fully automated in the space-based environment and have been proven to greatly improve layout designer productivity.
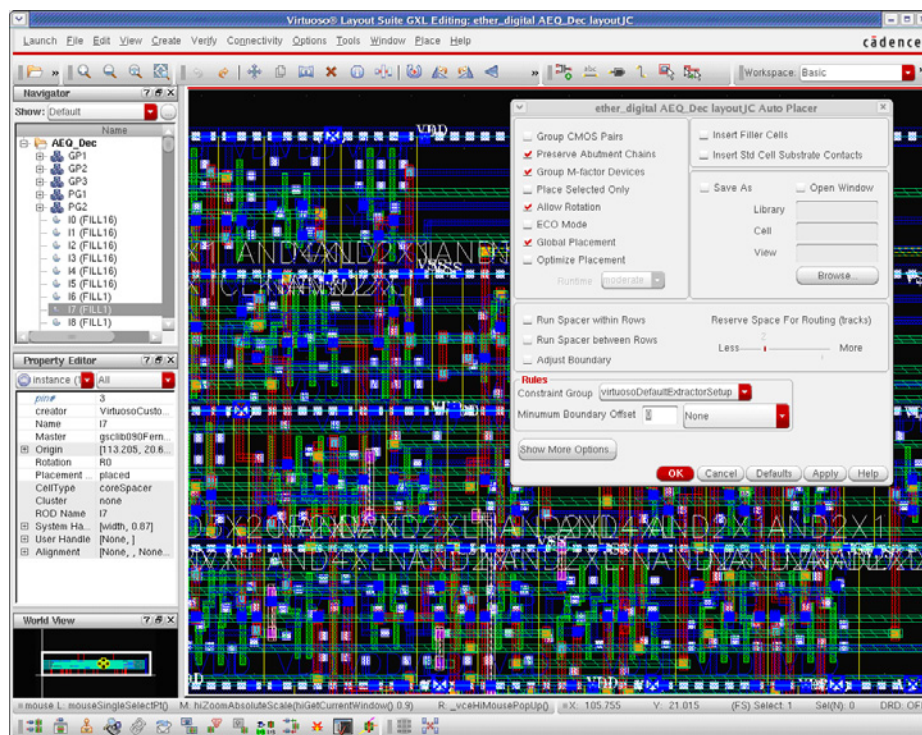

Figure 5: The Virtuoso custom-digital placer automatically places transistors, devices, and cells in block- and cell-based designs using more traditional row-based techniques

insert dummy devices, body contacts, and guard rings. The ability to generate these complex interdigitation patterns can be achieved in two ways—a user-friendly form for large arrays or interactively for minor edits to the array. Finally, users control the routing style and generate internal routing geometry.

Module generators can be created from either the schematic or the layout. When users create a MODGEN from the schematic, a MODGEN constraint is inserted in the Virtuoso common constraint environment. This constraint is then enforced automatically when the layout is created.

FULL CUSTOM-ANALOG AND CUSTOM-DIGITAL PLACEMENT

Virtuoso Analog Placer is capable of a number of analog/RF-centric automatic placement functions. This includes the automatic creation of quick placements and more robust placements that support more packing, as well as functions to fix DRC errors in the placement and adjust cell pins and sides. Virtuoso Analog Placer offers three modes of operation:

- Quick placement mode, which provides fast, DRC-aware placement for quick area estimation
- Quick placement as schematic mode, which provides placement-based device ordering in the schematic
- Fully automated placement with user-definable effort levels

The Cadence custom-digital placer automatically places transistors, devices, and cells in block- and cell-based designs using more traditional row-based methods. This placer is interoperable with Virtuoso Analog Placer and preserves MODGENs and user-defined groups.

YIELD OPTIMIZATION

Virtuoso Yield Optimizer is used for design-for-yield (DFY) optimization, which primarily involves the enforcement of recommended rules while maintaining all hierarchy, mandatory design rules, and design constraints such as symmetry and design-rule overrides. Users can

Virtuoso Layout Suite features	L	XL	GXL
OpenAccess database	•	•	•
Multi-tab support	•	•	•
Bookmarks and history	•	•	•
World View Assistant	•	•	•
SKILL Pcells	•	•	•
Qcells	•	•	•
Design-rule–driven editing	•	•	•
Search Assistant	•	•	•
Property Editor Assistant	•	•	•
32nm rule support	•	•	•
Information balloons	•	•	•
High-altitude selection	•	•	•
Dynamic measurement	•	•	•
Store/Restore selection set	•	•	•
Encounter interoperability on OA	•	•	•
SKILL integrated design environment	•	•	•
DRC fixing and compaction	•	•	•
Express Pcells	•	•	•
Annotation browser	•	•	•
Connectivity aware		•	•
Common constraint environment		•	•
Constraint-aware design		•	•
Wire editor, point-to-point router		•	•
Configurable hierarchy manager		•	•
Dynamic selection		•	•
Process rules editor		•	•
Synchronous cloning		•	•
Flexible token-based licensing			•
Analog Device Placer			•
Digital Device Placer			•
Module generation			•
Cell planning			•
Virtuoso Chip Assembly Router			•
Virtuoso Space-Based Router			•
Floorplanning			•
Cell and block placer			•
Yield optimization			•
Layout migration			•

also provide the hotspots and guidelines as output from litho simulation via HIF files and Virtuoso Yield Optimizer will automatically fix the litho violations.

DESIGN MIGRATION

Virtuoso Layout Migrate enables fast migration of a given design to a new or altered process geometry. Integrated with the Virtuoso platform, it provides hierarchical, two-dimensional optimization algorithms to achieve significantly higher quality of results (QoR) than traditional methods using near-linear shrinks.

INTERACTIVE DRC FIXING

Interactive DRC fixing is used for strategically fixing DRC errors in the layout in an automated fashion. This out-of-the-box technology runs natively on a Virtuoso OpenAccess technology file. The patented technology incrementally loads portions of the layout so that it can handle very large designs.

SPECIFICATIONS

THIRD-PARTY SUPPORT

- OpenAccess-compatible tools and functions
- PDKs (please contact your foundry provider for more information)

DESIGN INPUT

- OpenAccess database
- SKILL
- STREAM format
- OASIS format
- Cadence Chip Assembly Router database format

DESIGN OUTPUT

- OpenAccess database
- SKILL
- STREAM format
- OASIS format
- Cadence Chip Assembly Router database format

PLATFORM/OS

- Sun/Solaris
- HP-UX
- IBM AIX
- Linux

CADENCE SERVICES AND SUPPORT

- Cadence application engineers can answer your technical questions by telephone, email, or Internet—they can also provide technical assistance and custom training
- Cadence certified instructors teach more than 70 courses and bring their real-world experience into the classroom
- More than 25 Internet Learning Series (iLS) online courses allow you the flexibility of training at your own computer via the Internet
- Cadence Online Support gives you 24x7 online access to a knowledgebase of the latest solutions, technical documentation, software downloads, and more

For more information contact Cadence sales at:

+1.408.943.1234

or log on to:

www.cadence.com/ contact_us

cādence®

Cadence Design Systems, Inc.

CORPORATE HEADQUARTERS
2655 Seely Avenue
San Jose, CA 95134
P: +1.800.746.6223 *(within US)*
   +1.408.943.1234 *(outside US)*
F: +1.408.943.5001
www.cadence.com