DATASHEET

VIRTUOSO SCHEMATIC EDITOR L AND XL

FAST, EASY TO USE DESIGN AND CONSTRAINT ENTRY

The Cadence® Virtuoso® Schematic Editor family of products comprises the design and constraint composition environment that establishes the design intent of the industry-standard Virtuoso custom design platform, the complete solution for front-to-back custom-analog, digital, RF, and mixed-signal designs.

FAMILY OVERVIEW

The Virtuoso Schematic Editor product family provides the most comprehensive and flexible array of design and constraint composition capabilities that speed design and constraint entry and establish the design intent for the rest of the design and implementation tools. From abstracted architectural definitions, using industry-standard hardware description languages such as Verilog® and VHDL, to final structural schematic implementations at the transistor level, the Virtuoso Schematic Editor family helps designers implement each stage in their designs, while capturing and ensuring consistency of design intent with constraints.

The Virtuoso Schematic Editor product family is integrated with the Virtuoso Analog Design Environment, Virtuoso Multi-Mode Simulation, and Virtuoso Layout Suite to facilitate design convergence of front-to-back custom-analog, digital, RF, and mixed-signal design flows.

The Virtuoso Schematic Editor product family provides a flexible set of product performance levels, Virtuoso Schematic Editor L and Virtuoso Schematic Editor XL, to best suit your design flow needs. Virtuoso Schematic Editor L provides all the capabilities necessary to speed design entry on even the largest and most complex custom designs. Virtuoso Schematic Editor XL builds upon the L level, adding the first front-to-back unified common constraint environment as well as advanced features to facilitate design team collaboration.

FAMILY BENEFITS

- New, fast, easy-to-learn, easy-to-use design and constraint entry sets the design intent in one location
- Supports design abstraction by seamlessly integrating transistor schematics with language modules
- Features tight integration with other Cadence tools to speed design convergence

cadence®

- Increases productivity with new unified front-to-back common design environment
- Significantly speeds design entry, visualization, access, and control
- Lowers cost of support and maintenance with unified front-to-back design environment
- Flexible set of product levels supports a variety of design flows and needs
- Built-in design and language rule checking enables design problems to be found early
- Enables easy configuration and visualization of large, complex hierarchical designs
- Reduces risk by maintaining design intent between design specification and implementation with unified common constraint environment

FAMILY FEATURES AT A GLANCE:

Feature	L	XL
Multi-tab, multi-view canvas	•	•
Customizable workspaces	•	•
World View Assistant	•	•
Hierarchical schematics with support for Verilog, VHDL, and Verilog AMS	•	•
Hierarchical cross-probing front to back	•	•
Generate bookmarks and history	•	•
Expanded Search Assistant	•	•
Design Navigator Assistant	•	•
Property Editor Assistant	•	•
Updated common constraints		•
Constraint Manager Assistant		•
Automated constraint annotation on schematic		•
Circuit Prospector Assistant		•
Analog schematic generation from SPICE		•
HTML Design Publisher		•
Analog schematic generation from SPICE		•
Schematic to CPF model generator for Cadence low-power design flow		•

VIRTUOSO SCHEMATIC EDITOR L

PRODUCT OVERVIEW

Virtuoso Schematic Editor L is the design intent environment of the industry-standard Virtuoso custom design platform, the complete solution for front-to-back custom-analog, digital, RF, and mixed-signal design.

Virtuoso Schematic Editor L, which is built upon the new unified Virtuoso custom design platform, utilizes the latest advances in user interfaces and design tool integration to bring unprecedented levels of productivity and integration to design creation. The new unified Virtuoso custom design platform includes new capabilities and design flow enhancements such as modern, familiar, and user-customizable toolbars, icons, pull-down menus, a

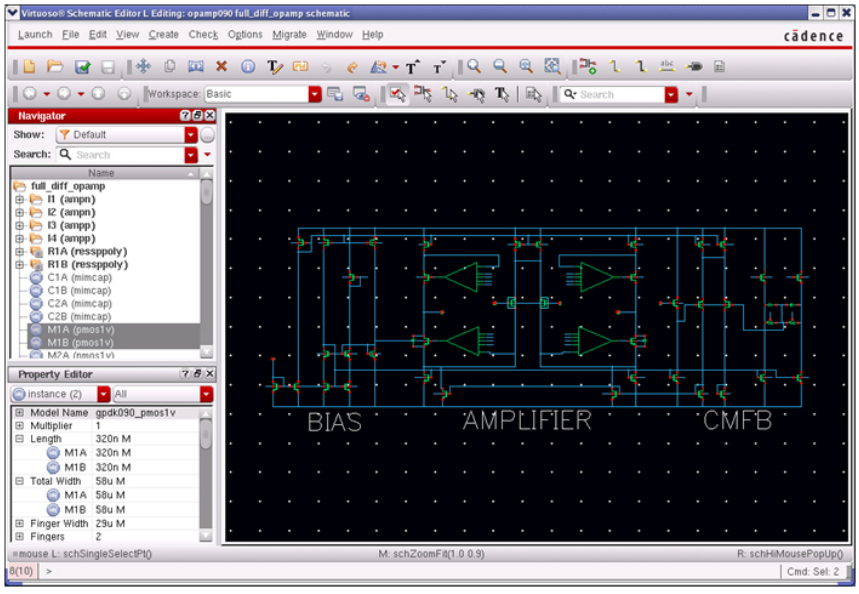

Figure 1: Virtuoso Schematic Editor L

multi-tab, multi-view design canvas, workspaces, bookmarks, history, and more (see Figure 1).

Virtuoso Schematic Editor L provides the most comprehensive and flexible array of design composition capabilities that can speed design entry on even the largest and most complex custom designs. From architectural definition, using industry-standard hardware description languages such as Verilog and VHDL, to final structural schematic implementations at the transistor level, Virtuoso Schematic Editor L helps designers implement each stage in their designs.

For larger and more complex block- and chip-level designs, Virtuoso Schematic Editor L not only supports multi-sheet designs but also provides the ability to design hierarchically with no limit on the number of levels used. The integrated Hierarchy Editor makes hierarchical designs easy to traverse, and automatically ensures that all connections are maintained accurately throughout the design.

Well-defined component libraries from the industry's broadest selection of PDKs, originated by the world's leading foundries, enable faster schematic design at both the gate and transistor levels for process nodes from 0.35um to 28nm and everything in between. Advanced wire routing capabilities further assist in connecting devices.

Virtuoso Schematic Editor L is integrated with the Virtuoso Analog Design Environment, Virtuoso Multi-Mode Simulation, and Virtuoso Layout Suite to provide a complete solution for front-to-back custom-analog, digital, RF, and mixed-signal design flows.

To better suit your design flow needs, Virtuoso Schematic Editor L also provides an easy path to the higher performance level and constraint composition capabilities of Virtuoso Schematic Editor XL.

BENEFITS

- New, fast, easy-to-learn, easy-to-use design entry
- Increased productivity with new unified front-to-back common design environment
- Significant speed improvements in design entry, visualization, access, and control
- Lower cost of support and maintenance with unified front-to-back design environment
- Flexible set of product levels to support a variety of design flows and needs
- Design problems found early with built-in design and language rule checking
- Easy visualization and configuration of large, complex hierarchical designs
- Rapid command execution with user-configurable bindkeys and menus
- Custom check tabs and associated rules checks
- Inherited connections limit the clutter associated with power and isolation connectivity nets
- Recognizes sophisticated device parameter interaction using Cadence SKILL callbacks

FEATURES

UNIFIED VIRTUOSO CUSTOM DESIGN PLATFORM

Virtuoso Schematic Editor L utilizes all of the new unified features of the Virtuoso custom design platform to facilitate fast and easy design entry. A modern common user cockpit for design creation is accompanied by familiar and user-customizable toolbars, icons, and pull-down menus. Location and content of toolbars are user-defined and saved in custom workspaces for the most efficient use of screen space depending on tasks. A multi-window, multi-tabbed canvas, bookmarks, and history define an intuitive editing environment, which allows users to open multiple schematics, or different views of the same design, and consequently manage their designs more quickly and effectively.

UNIFIED VIRTUOSO DESIGN TASK ASSISTANTS

The design task assistants can be docked or undocked, configured, and saved in multiple workspaces suited to each designer's styles and needs depending on the task at hand.

A native Navigator Assistant provides quick, efficient, and intuitive access to the complete design hierarchy and all design objects directly from within the schematic editing environment.

A native Search Assistant provides quick, efficient, and comprehensive search engine capabilities directly within the schematic editing environment. The Search Assistant automatically categorizes search results into logical groups, displaying common items in a familiar tree structure. This makes it very easy for users to find and access information within the design, the design libraries, menu commands, and even the Cadence SKILL programming language. Context-sensitive menus and double-click operations allow for rapid operations on selected results.

A modern Property Editor Assistant docked around the main schematic editing canvas, or undocked and placed anywhere on a user's workstation, allows fast, efficient, and intuitive editing of multiple properties on a single design object or multiple design objects. New multi-color visual display and coding of property values rapidly identifies common and varying property settings.

FAST AND ACCURATE DESIGN ENTRY

Virtuoso Schematic Editor L has many features that facilitate fast and easy design entry. First among these capabilities, a well-defined component library—which is integrated with the product—enables fast design at both the gate and transistor level. This feature is complemented with sophisticated wire routing capabilities to assist in connecting devices. For larger and more complex designs, Virtuoso Schematic Editor L supports both multi-sheet designs and the ability to design hierarchically, with no limit to the number of levels used. Hierarchical designs are easy to traverse using the Hierarchy Editor, and

Virtuoso Schematic Editor L ensures that all connections are maintained accurately throughout a design.

DESIGN WITH INDUSTRY STANDARD LANGUAGES

Virtuoso Schematic Editor L is well suited for entering mixed-level designs, using descriptions based on the industry's two leading hardware description languages—VHDL and Verilog HDL. It also supports the ability to use Verilog-AMS and VHDL-AMS mixed-signal languages, thereby providing a standard way of entering designs regardless of design type. In addition to entering these languages, the user has the ability to generate block representations from the HDL descriptions automatically, facilitating a system-level approach to IC design.

EXTENSIVE DESIGN CHECKING CAPABILITIES

User-configurable rule checks identify drawing and electrical rule violations, such as overlapping components, open or shorted connections, unconnected inputs and outputs, object consistency, and illegal names to ensure the accuracy of your design. It allows the designer to check connections throughout the entire design hierarchy for pin name matches, completion of wire connections, and proper wire labeling. The designer has the flexibility of checking individual pages of a design, or checking the entire design hierarchy with one command. Users can create custom tab and associated rules checks for schematic rules check.

COMPREHENSIVE INTEGRATION—CROSS-APPLICATION CAPABILITIES

Virtuoso Schematic Editor L is the complete single source for all connectivity-driven design, verification, and implementation needs. In conjunction with Virtuoso Analog Design Environment, Virtuoso Multi-Mode Simulation, and Virtuoso Layout Suite, Virtuoso Schematic Editor L provides cross-application hierarchical browsing, selection, and backannotation. Connectivity and device parameters are checked for correctness using construction layout implementation. Bi-directional incremental updates are provided for complete engineering change order (ECO) control.

VIRTUOSO SCHEMATIC EDITOR XL

PRODUCT OVERVIEW

Virtuoso Schematic Editor XL is the new design and constraint composition environment of the industry-standard Virtuoso custom design platform, the complete solution for front-to-back custom-analog, digital, RF, and mixed-signal design.

Built upon the new unified Virtuoso custom design platform, and utilizing the latest advances in user interface and design tool integration, Virtuoso Schematic Editor XL includes all of the updated capabilities and design flow enhancements of Virtuoso Schematic Editor L with the added unified common constraint composition environment, bringing even higher levels of productivity to design creation and design team communication.

The new unified Virtuoso common constraint environment is the first to capture, manage, and visualize critical custom design constraints, as well as being the first to formalize communication between design, verification, and implementation teams. Electrical and physical constraints are captured directly alongside connectivity in schematics to fully define a design's intent, leading to the formation of a complete design specification. This formal specification is used side by side with schematic-driven design to complete the first constraint-driven design environment. Interactive, assisted, and automated modes also aid in the formal signoff of constraint specifications (see Figure 2).

Virtuoso Schematic Editor XL also inherits from the L tier all the modern, familiar and user-customizable toolbars, icons, pull-down menus, multi-tab multi-view canvas, workspaces, bookmarks, history, and more. It also delivers the most comprehensive and flexible array of design composition capabilities that can speed design entry on even the largest and most complex custom designs. From architectural definition, using industry-standard hardware description languages such as Verilog and VHDL, to final structural schematic implementations at the transistor level, Virtuoso Schematic Editor XL not only helps you implement each stage in your design, it also maintains design intent throughout your flow.

Virtuoso Schematic Editor XL operates with the same well-defined component libraries—from the industry's broadest selection of PDKs coming out of the world's leading foundries—for process nodes from 0.35um to 28nm and everything in between, allowing for faster schematic design at both the gate and transistor levels.

Virtuoso Schematic Editor XL is integrated with Virtuoso Analog Design Environment, Virtuoso Multi-Mode Simulation, and Virtuoso Layout Suite for the complete solution for front-to-back schematic and constraint-driven custom-analog, digital, RF, and mixed-signal design flows.

BENEFITS

- New, fast, easy-to-learn, easy-to-use design and constraint entry
- CPF model generation to support the Cadence low-power design flow
- Design publishing to facilitate design reviews over the web
- Reduce risk by maintaining design intent between design specification and implementation
- Facilitate design reuse by capturing the design process as IP
- Easy design reviews with integral documentation, specifications, measurement results, and waveforms
- Easily communicate critical design constraints between multiple users and sites
- Formally manage, verify, and signoff critical design constraints
- Increased productivity and design quality with constraint- and design-rule driven features to automatically ensure design and process correctness in real time
- Increased productivity with new unified front-to-back common design environment
- Significant speed improvements in design entry, visualization, access, and control
- Lower cost of support and maintenance with unified front-to-back design environment
- Flexible set of product levels to support a variety of design flows and needs
- Design problems found early with built-in design and language rule checking
- Easy visualization and configuration of large, complex hierarchical designs
- Rapid command execution with user-configurable bindkeys and menus
- Inherited connections limit the clutter associated with power and isolation connectivity nets
- Recognizes sophisticated device parameter interaction using Cadence SKILL callbacks

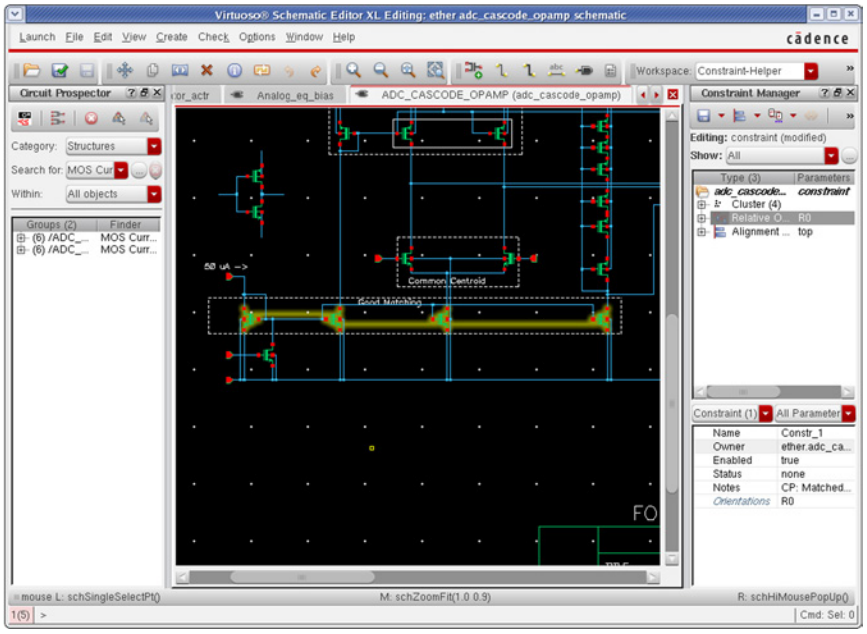

Figure 2: Virtuoso Schematic Editor XL common constraint environment

FEATURES

UNIFIED VIRTUOSO CUSTOM DESIGN PLATFORM

Virtuoso Schematic Editor XL uses all of the unified features of the Virtuoso custom design platform to facilitate fast and easy design entry. A modern common user cockpit for design creation is accompanied by familiar and user-customizable toolbars, icons, and pull-down menus. The location and content of toolbars can be defined by the user and saved in custom user workspaces for the most efficient use of screen space, depending upon the particular tasks undertaken. A multi-window multi-tabbed canvas, bookmarks, and history define an intuitive editing environment, which allows users to open multiple schematics, or different views of the same design, and consequently manage their designs more quickly and effectively.

UNIFIED VIRTUOSO COMMON CONSTRAINT ENVIRONMENT

Virtuoso Schematic Editor XL introduces the first unified common constraint environment comprising of a comprehensive suite of constraint capture, editing, visualization, management, and verification functionality. Interactive, assisted and automated circuit prospecting, constraint templates and constraint generation aid in speeding the formal capture and signoff of constraint specifications preserving and ensuring designer's intent on critical designs. Common circuit structures and topologies are built-in for automatic identification or prospecting, as well user-definable circuit structures and topologies, which are easily added to create an expanded set of circuit structures and constraints. Additionally, as done with schematics, constraints are captured as design IP to facilitate reuse.

UNIFIED VIRTUOSO DESIGN TASK ASSISTANTS

Virtuoso Schematic Editor XL includes a suite of new unified front-to-back custom design task assistants that speed common creation, editing, checking, browsing, search, and design traversal tasks by as much as 5x over Virtuoso Schematic Editor L. The design task assistants can be docked or undocked, configured, and saved in multiple workspaces suited to each designer's styles and needs depending on the task at hand.

A native Navigator Assistant provides quick, efficient, and intuitive access to the complete design hierarchy and all design objects directly from within the schematic editing environment.

A native Search Assistant provides quick, efficient, and comprehensive search engine capabilities directly within the schematic editing environment. The Search Assistant automatically categorizes search results into logical groups, displaying common items in a familiar tree structure, making it very easy for users to find and access information within the design, the design libraries, menu commands, and even the Cadence SKILL programming language. Context-sensitive menus and double-click operations allow for rapid operations on selected results.

A modern Property Editor Assistant docked around the main schematic editing canvas, or undocked and placed anywhere on a user's workstation, allows fast, efficient, and intuitive editing of multiple properties on a single design object or multiple design objects. New multi-color visual display and coding of property values rapidly identifies common and varying property settings.

A new Annotation Browser brings an easy-to-use interface to design and design object browsing while debugging common schematic and connectivity error markers.

FAST AND ACCURATE DESIGN ENTRY

Virtuoso Schematic Editor XL has many features that facilitate fast and easy design entry. These capabilities start with well-defined component libraries—which are integrated with the product—that allow for fast design at both the gate and transistor levels. This feature is complemented with sophisticated wire-routing capabilities to assist in connecting devices. For larger and more complex designs, Virtuoso Schematic Editor XL supports both multi-sheet designs and the ability to design hierarchically, with no limit to the number of levels used. Hierarchical designs are easy to traverse using the Hierarchy Editor, and Virtuoso Schematic Editor XL ensures that all connections are maintained accurately throughout the design.

DESIGN WITH INDUSTRY STANDARD LANGUAGES

Virtuoso Schematic Editor XL is well suited for entering mixed-level designs, using descriptions based on the industry's two leading hardware description languages—VHDL and Verilog HDL. It also supports the ability to use Verilog-AMS and VHDL-AMS mixed-signal languages, thereby providing a standard way of entering designs regardless of design type. In addition to entering these languages, the user has the ability to generate block representations from the HDL descriptions automatically, facilitating a system-level approach to IC design.

EXTENSIVE DESIGN CHECKING CAPABILITIES

To ensure the accuracy of designs, user-configurable rule checks identify drawing and electrical rule violations, such as overlapping components, open or shorted connections, unconnected inputs and outputs, object consistency, and illegal names. This capability allows the designer to check connections throughout the entire design hierarchy for pin name matches, completion of wire connections, and proper wire labeling. The designer also has the flexibility of checking individual pages of the design, or checking the entire design hierarchy with one command.

COMPREHENSIVE INTEGRATION—CROSS-APPLICATION CAPABILITIES

Virtuoso Schematic Editor XL comprises the complete single source for all connectivity-driven design, verification, and implementation needs. In conjunction with Virtuoso Analog Design Environment, Virtuoso Multi-Mode Simulation, and Virtuoso Layout Suite, Virtuoso Schematic Editor XL provides cross-application hierarchical browsing, selection, and back annotation. Connectivity and device parameters are checked for correctness using construction layout implementation. Bi-directional incremental updates are provided for complete ECO control.

SPECIFICATIONS

DESIGN COMPOSITION

- Unlimited design hierarchy support
- Simplified automatic generation of an HDL template
- Support of multi-sheet schematics
- HTML publisher for schematics
- Power Intent Export Assistant, to specify power intent of the design
- User-configurable command bindkeys and label display
- Dynamic highlighting for easy design correction
- Automated interactive connection router
- User-configurable selection with filtering
- Comprehensive symbol creation and editing features
- User-configurable undo/redo levels
- Move, copy, stretch, rotate, and delete editing options
- Search and replace features
- Customizable tool environment using Cadence SKILL
- Online help system using HTML/PDF formatted publications

DESIGN CHECKING

- Schematic or symbol cell views checked individually
- Entire design hierarchy checked with one command
- Connectivity and consistency checks across pages and hierarchy
- Schematic rules checker (SRC) makes both logical and physical checks

DESIGN INPUTS

- CDL netlist
- EDIF 2 0 0 netlist
- SPICE netlist

- VHDL IEEE 1076-1993
- Verilog IEEE 1364
- Cadence SKILL

DESIGN OUTPUTS

- CDL netlist
- EDIF 2 0 0 netlist
- SPICE netlist
- VHDL IEEE 1076-1993
- Verilog IEEE 1364

HW/COMPUTING PLATFORM/OS

- Sun/Solaris
- HP-UX
- IBM AIX
- Linux

CADENCE SERVICES AND SUPPORT

- Cadence application engineers can answer your technical questions by telephone, email, or Internet—they can also provide technical assistance and custom training
- Cadence certified instructors teach more than 70 courses and bring their real-world experience into the classroom
- More than 25 Internet Learning Series (iLS) online courses allow you the flexibility of training at your own computer via the Internet
- Cadence Online Support gives you 24x7 online access to a knowledgebase of the latest solutions, technical documentation, software downloads, and more

For more information contact Cadence sales at:

+1.408.943.1234

or log on to:

www.cadence.com/cadence/contact_us

cadence®

Cadence Design Systems, Inc.

CORPORATE HEADQUARTERS
2655 Seely Avenue
San Jose, CA 95134
P: +1.800.746.6223 *(within US)*
+1.408.943.1234 *(outside US)*
F: +1.408.943.5001
www.cadence.com

21928 03/11 IW/MK/DM/PDF